

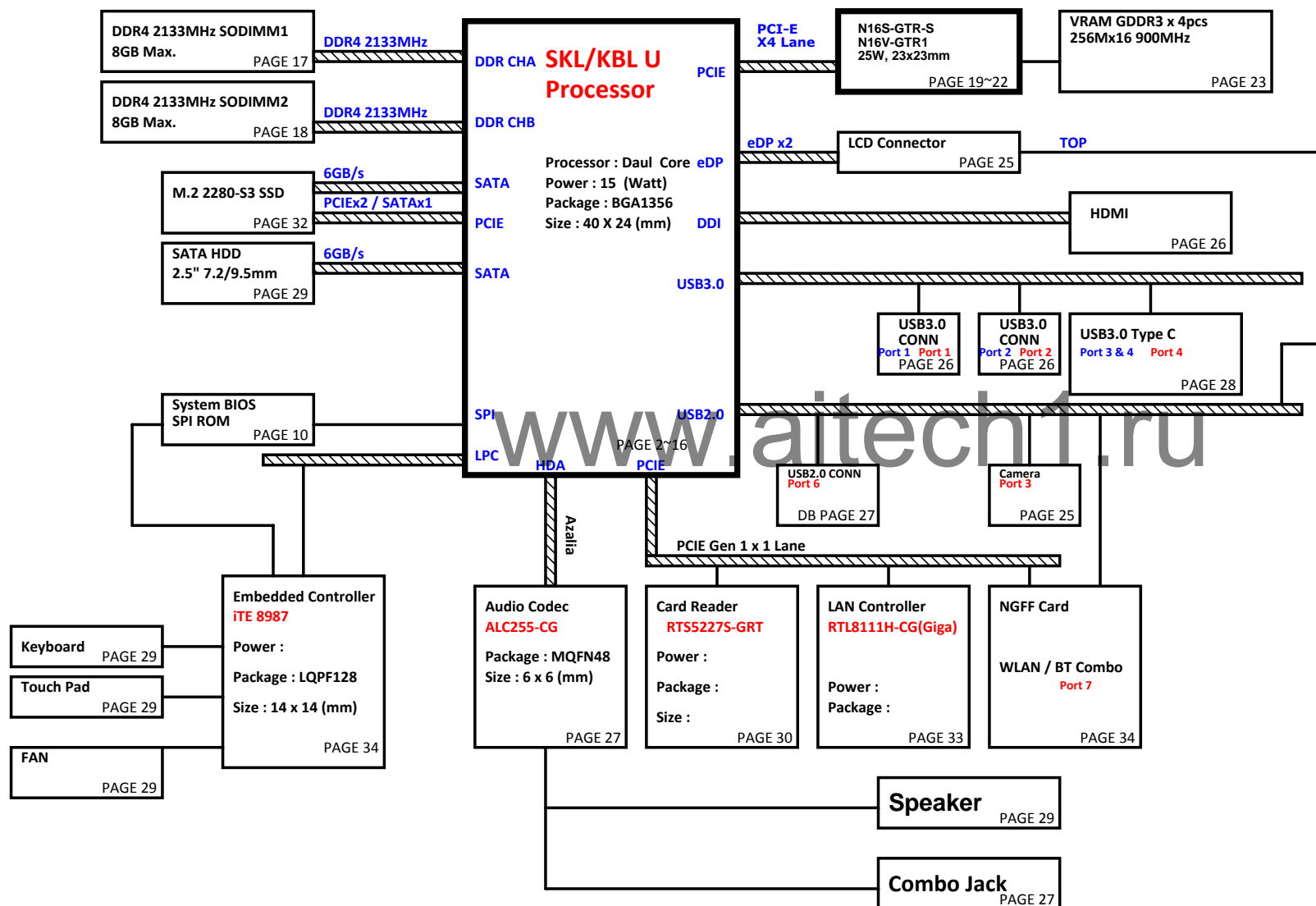
DIS (15")

LG9

Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

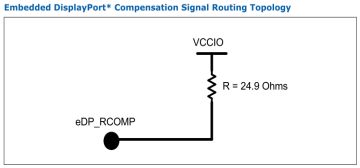
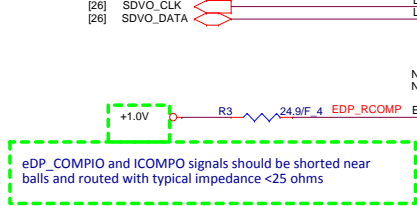
LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT



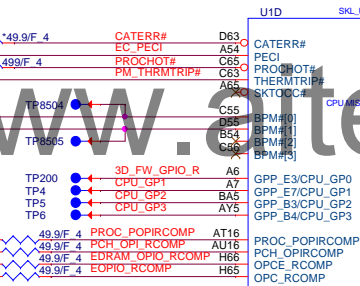
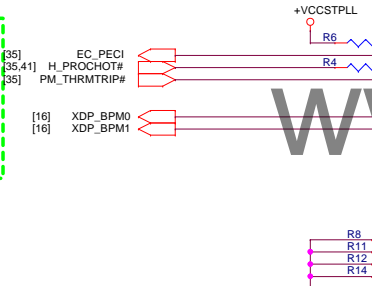
HDMI I.4

	+3V	[4,10,13,15,21,25,27,29,30,32,33,35,41,45,46]
	+1.0V	[4,6,16,34,35,40]
	+VCCSTPLL	[4,6,9,13,40,41]
DDPB_CTRLCLK	If using HDMI* , 2.2 K Ω \pm 5% pull-up to 3.3 V before HDMI* level shifter. and 2.2 K Ω \pm 5% pull-up to 5V after the level shifter.	
DDPB_CTRLDATA	This signal needs to be pulled up through a 2.2K Ω \pm 5% pull-up to 3.3V to enable Port B. For HDMI*, 2.2 K Ω \pm 5% pull-up to 3.3V before HDMI* level shifter and 2.2 K Ω \pm 5% pull-up to 5V after the level shifter is required.	

0317 CQ
Del R868 & R869 2.2K PU +3V (重複)



Close to EC
+VCCSTPLL
1K_4
R5
PM_THRMTRIP#
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL.
470 OHM IS FOR I/P



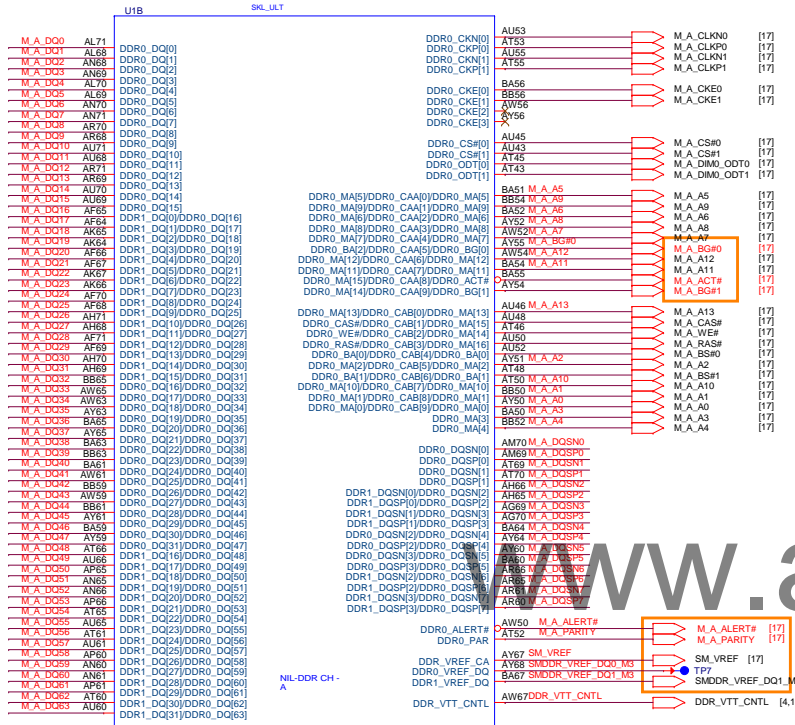
SkyLake ULT Processor (DDR4)

Non-Interleave / side by side

[17] M_A_DQS#(7:0)
[17] M_A_DQS#(7:0)
[18] M_B_DQS#(7:0)
[18] M_B_DQS#(7:0)
[17] M_A_DQ#(3:0)
[18] M_B_DQ#(3:0)

[6,17,18,38,40,48] +1.2V/SUS

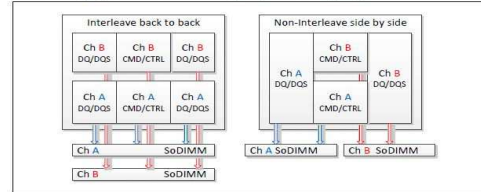
Need apply PN



*SKL_ULT
REV = 1

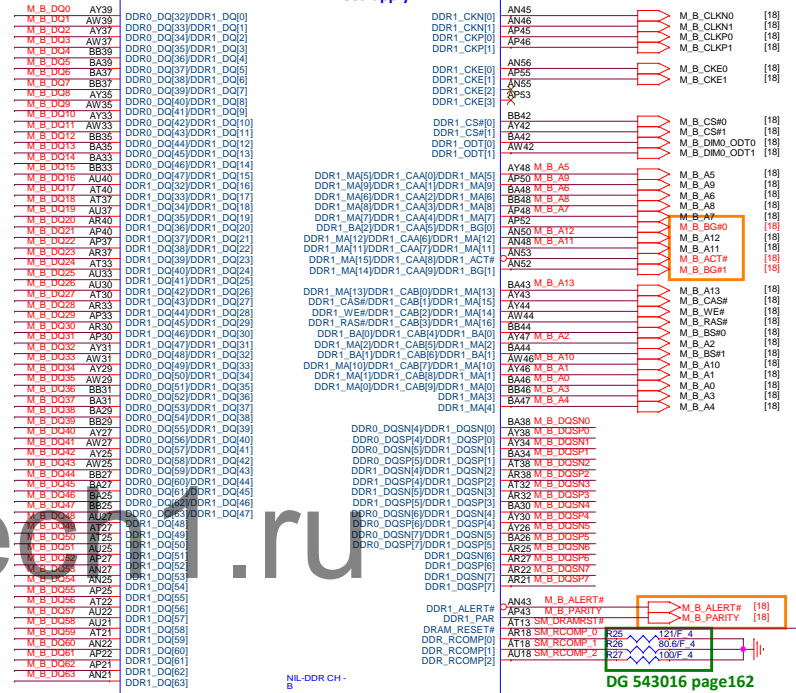
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Interleave (IL) and Non-Interleave (NIL) Modes Mapping




U1C SKL_ULT

Need apply PN



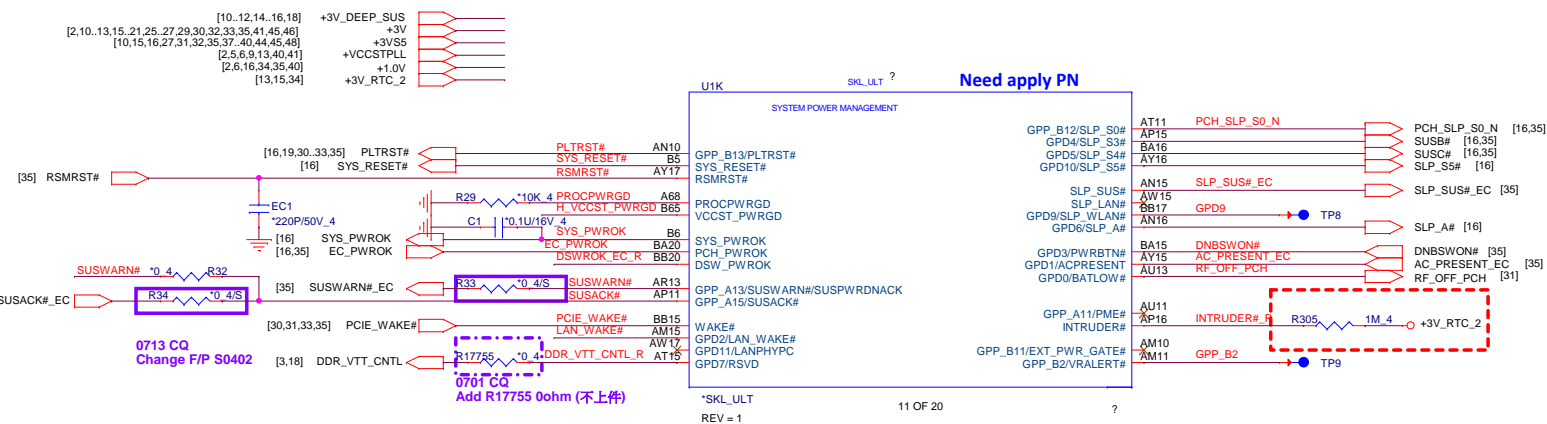
*SKL_ULT
REV = 1

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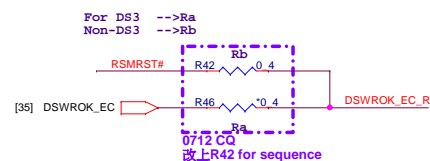
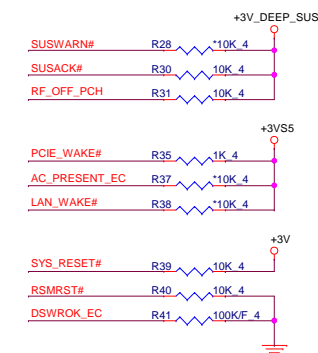


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Quanta Computer Inc.

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Custom	SKL-02 [DDR4]	1A
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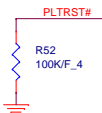


PCH Pull-high/low(CLG)

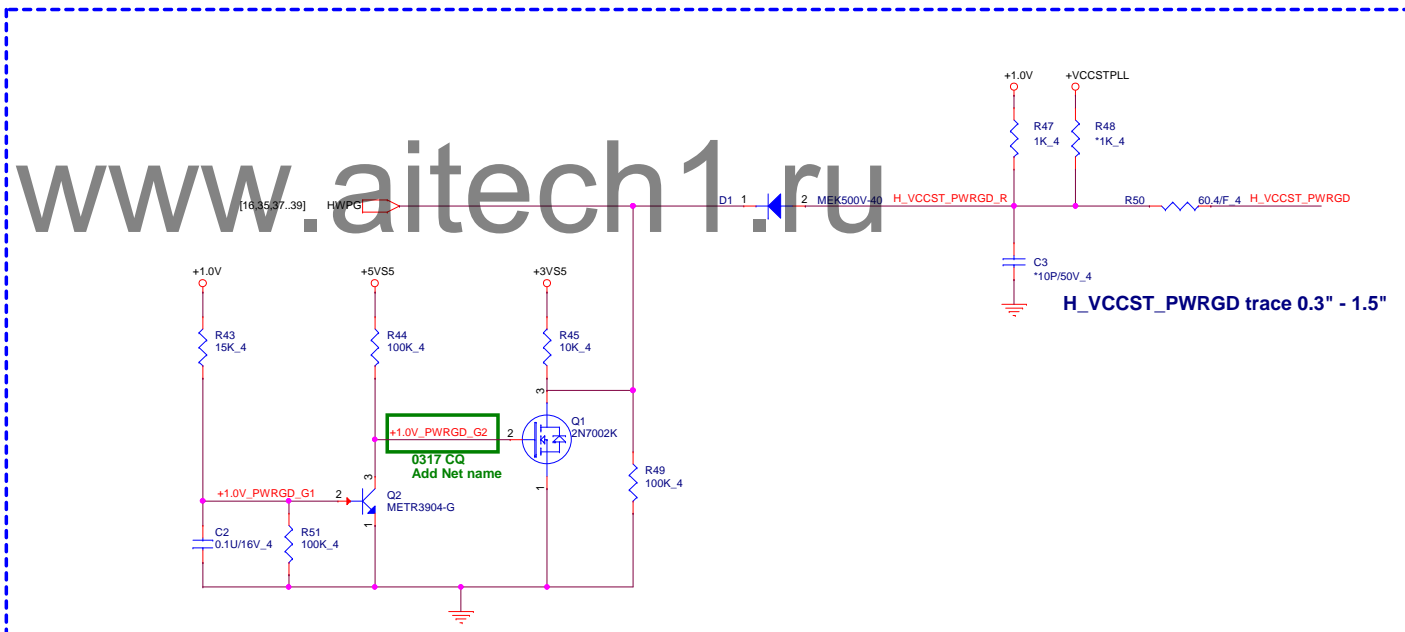
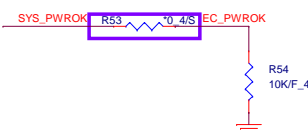


PLTRST#(CLG)

Rise/Fall time less than 100ns

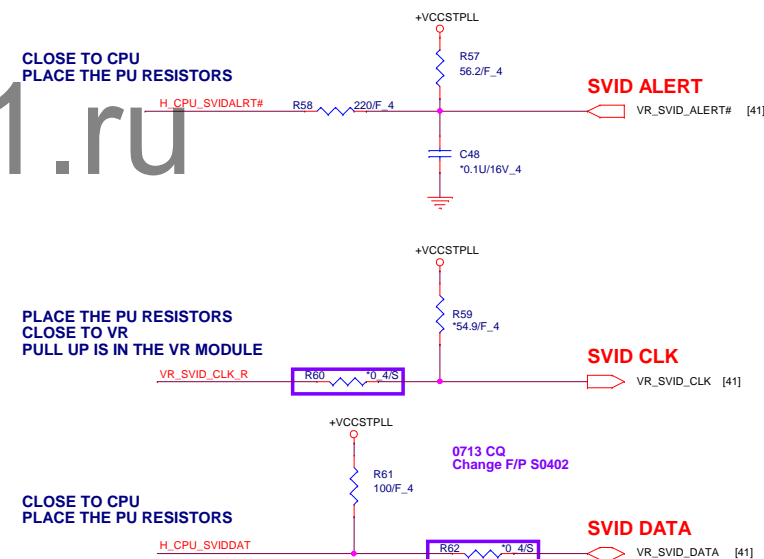


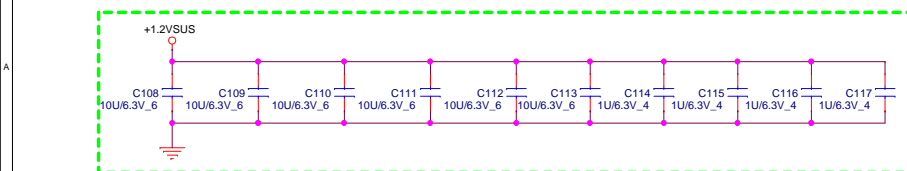
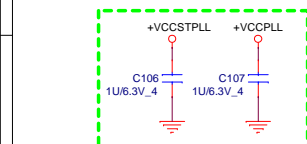
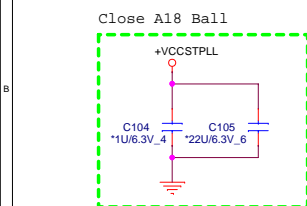
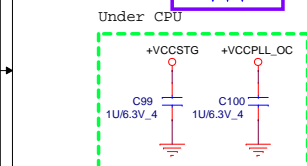
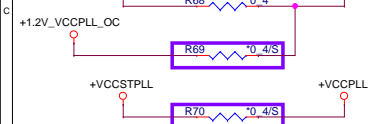
System PWR_OK(CLG)



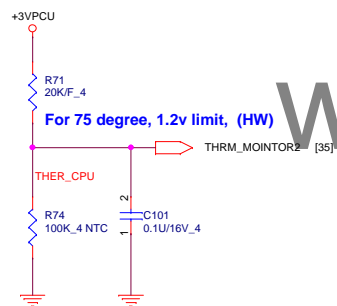


Layout note: need routing together and ALERT need between CLK and DATA



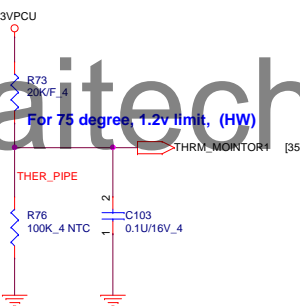


For CPU USE



For 75 degree, 1.2v limit, (HW)

IO Thrm Protect



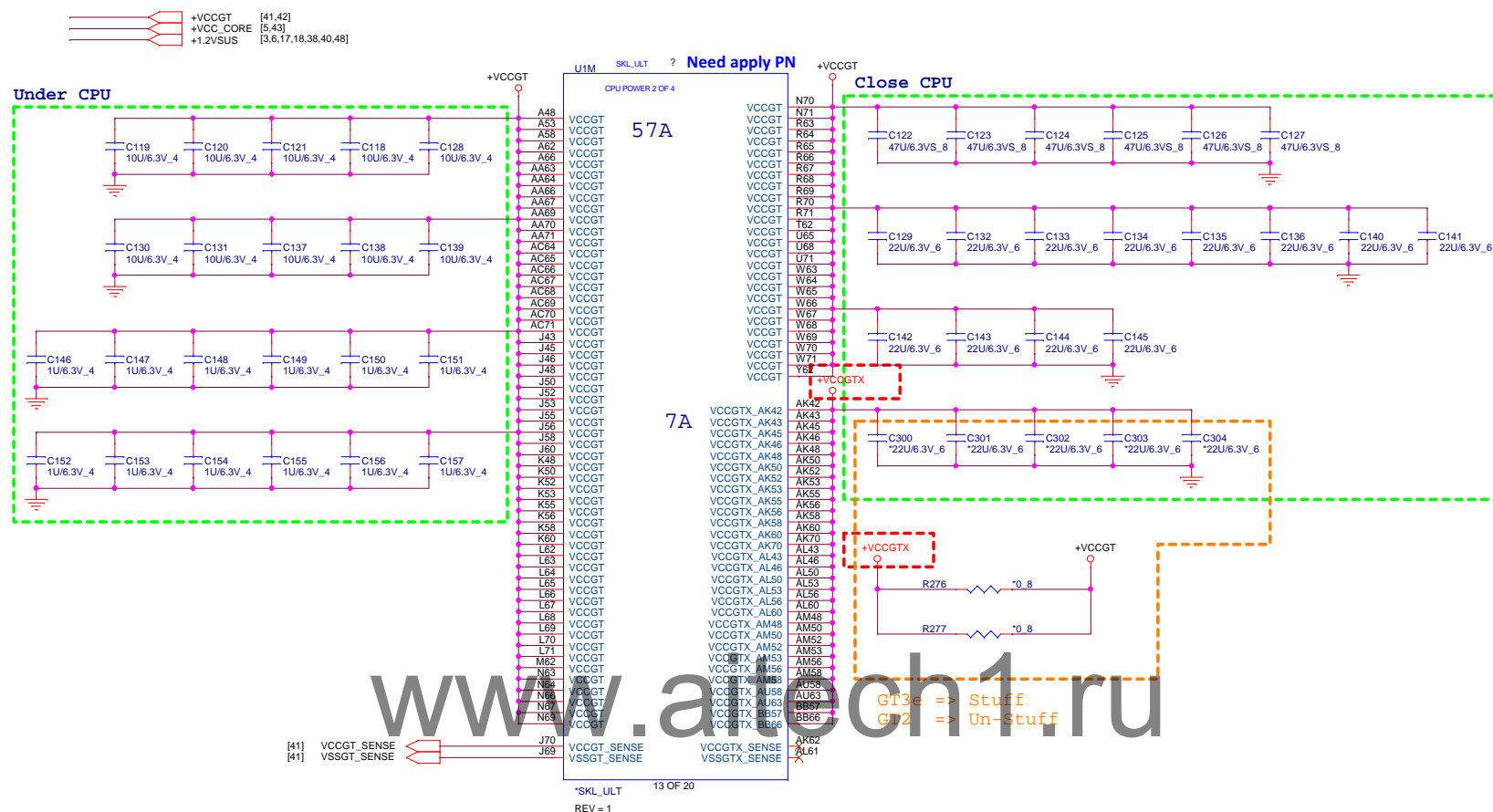
For 75 degree, 1.2v limit, (HW)

Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

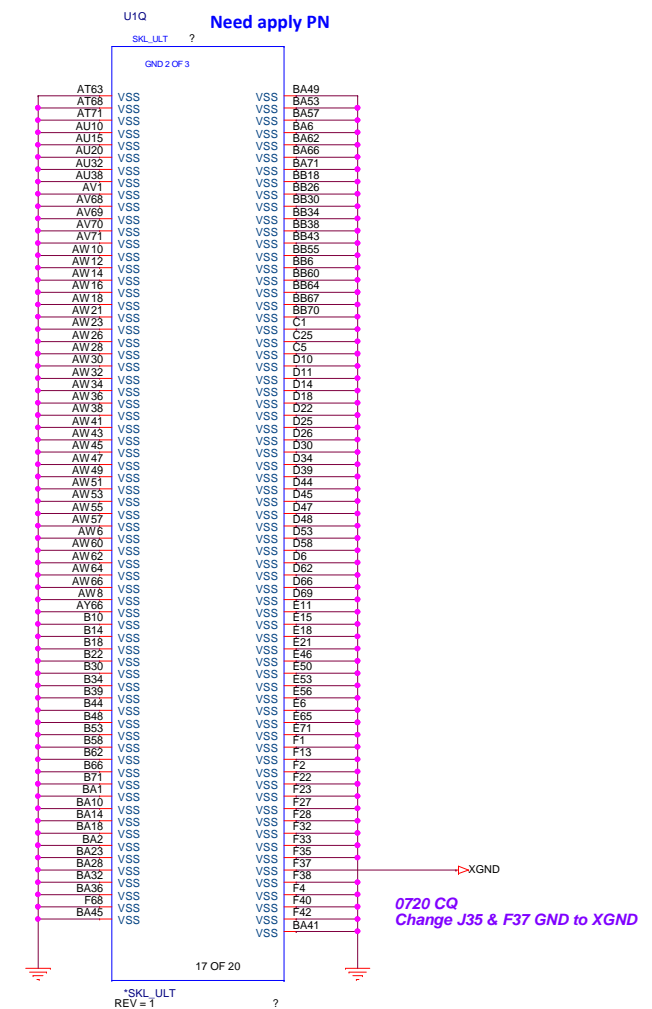
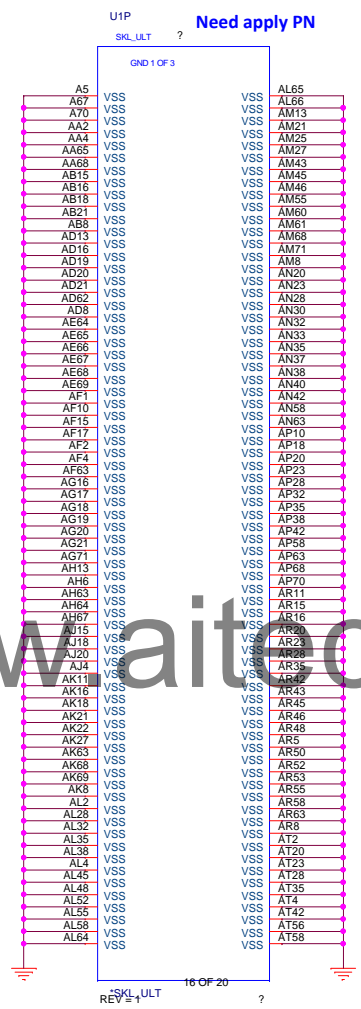
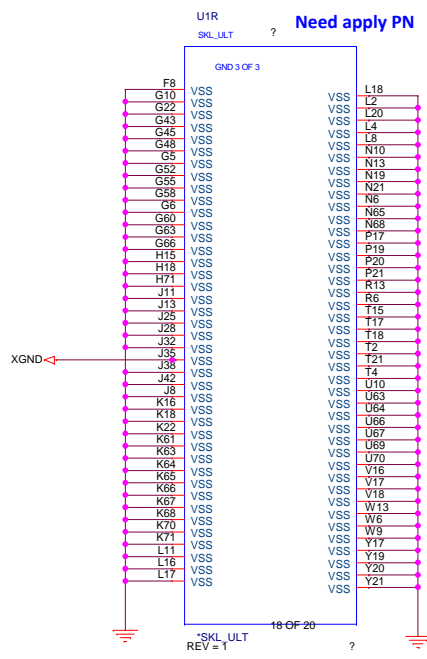


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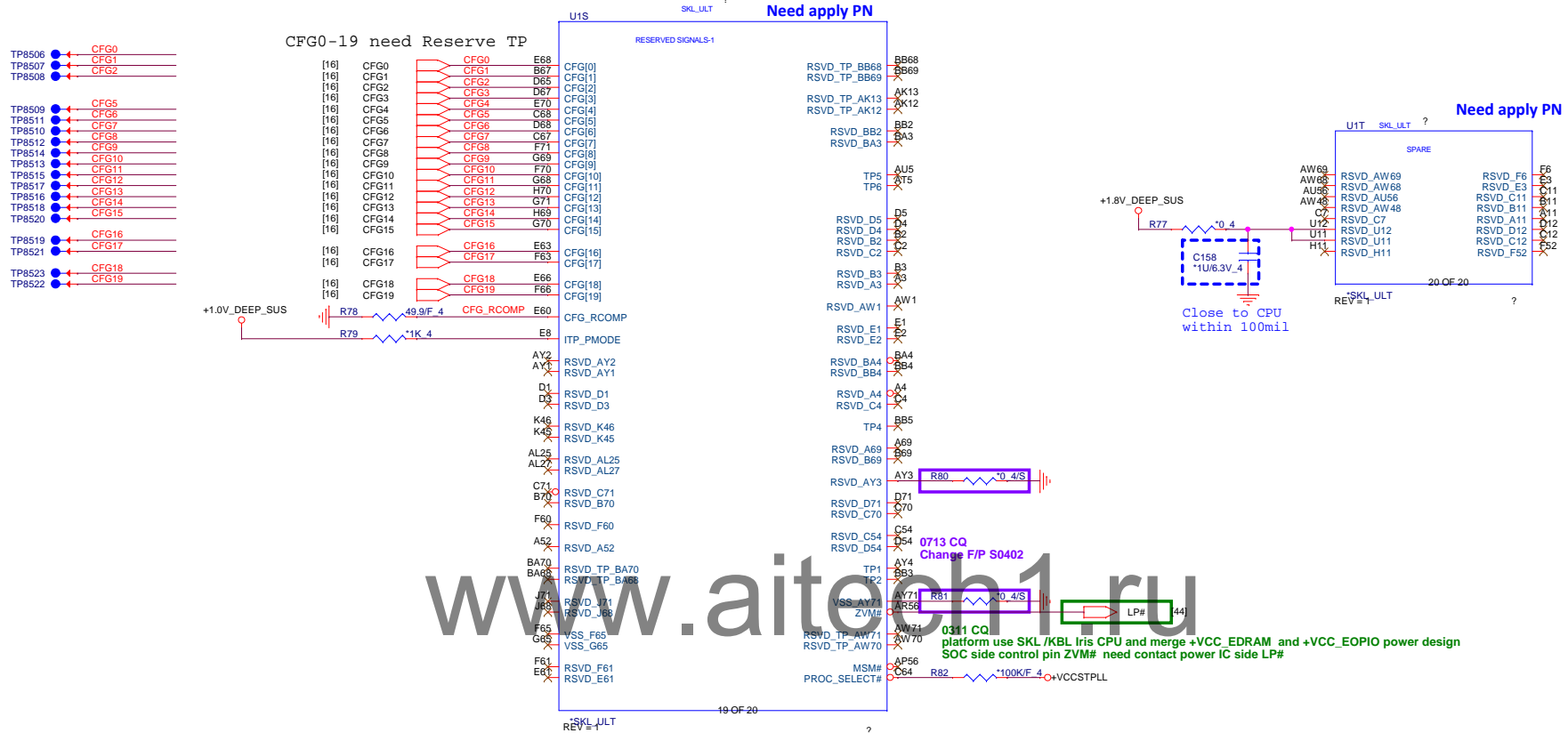


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



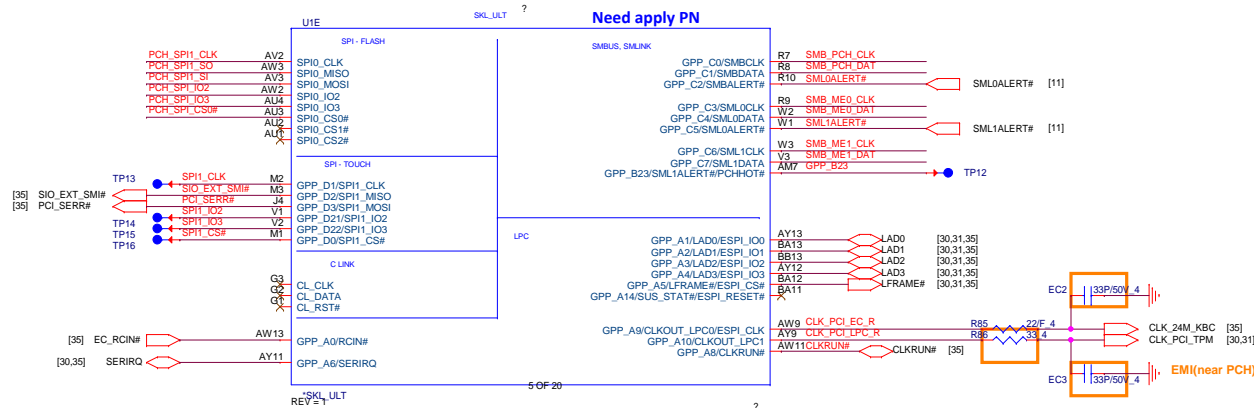
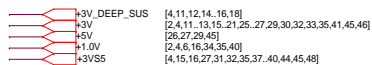
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[5,15,39] +1.8V_DEEP_SUS
[15,16,39,40] +1.0V_DEEP_SUS

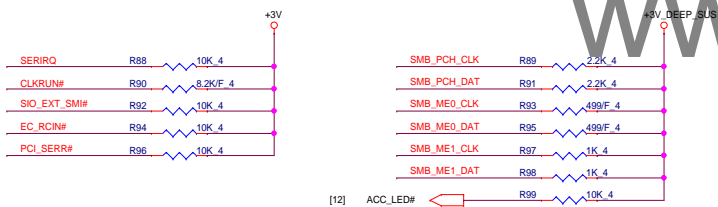


Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 *1K 4



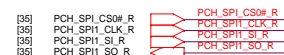
GPIO Pull UP



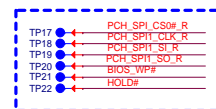
PCH SPI ROM(CLG)

3/31 CQ
Fix ROM PN

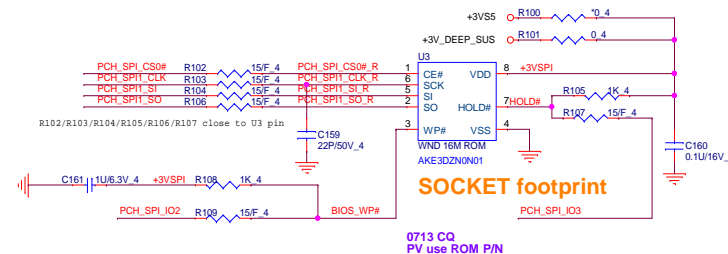
Vendor	Size	P/N
Winbond	16MB	AKE3DZN0N01 - IC FLASH(8P) W25Q128FVSIQ(SOIC)
GGD	16MB	AKE3DF00Q00 - IC FLASH(8P)GD25B128CSIGR(SOP)
Socket		DFHS08FS023



need place to TOP

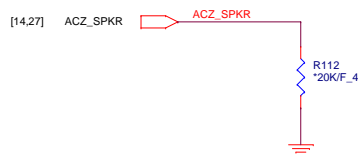


PCH SPI ROM(CLG)

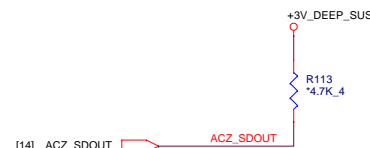


Functional Strap Definitions

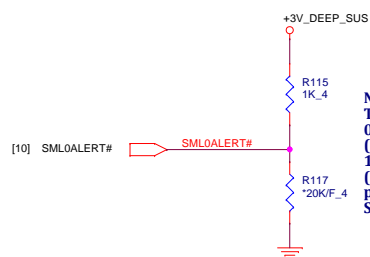
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



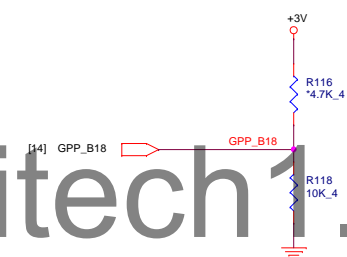
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



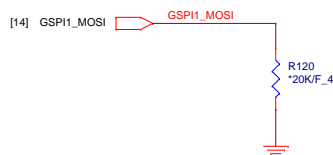
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



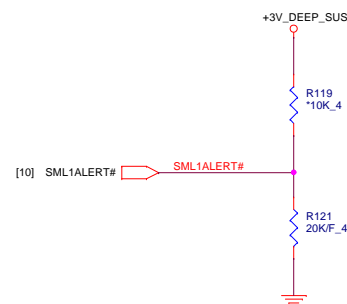
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



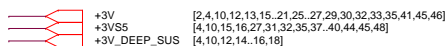
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



[2,4,10,12,13,15..21,25..27,29,30,32,33,35,41,45,46]
[4,10,15,16,27,31,32,35,37..40,44,45,46]
[4,10,12,14..16,18]

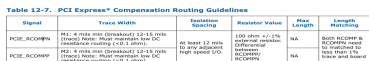


Table 12-7. PCI Express® Compensation Routing Guidelines

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length	Length Hatching
PCIE_RCOMP _N	M1: 4 mils min (breakout) 12-15 mils (trace) Must maintain low DC resistance routing (C = 1 nF)	At least 12 mils to any adjacent high speed I/O.	100 ohm +/- 1% external resistor. Differential pair.	NA	Both RCOMP _N and RCOMP _P need to be matched to less than 1% trace and board
PCIE_RCOMP _P	M2: 4 mils min (breakout) 12-15 mils (trace) Must maintain low DC resistance routing (C = 1 nF)		100 ohm +/- 1% external resistor. Differential pair.	NA	

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	NA
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	CardReader
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8			
Port9	WLAN		
Port10			
Port11			
Port12	SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 TYPE C
PORT-4	USB3.0 TYPE C

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 MB-2
PORT-3	Camera
PORT-4	Cobime USB3.0 TYPE C
PORT-5	NC
PORT-6	USB2.0 MB
PORT-7	WLAN
PORT-8	NC
PORT-9	NC
PORT-10	NC



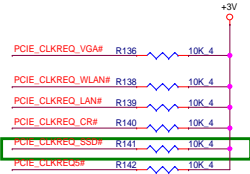
PROJECT : LG9
Quanta Computer Inc.

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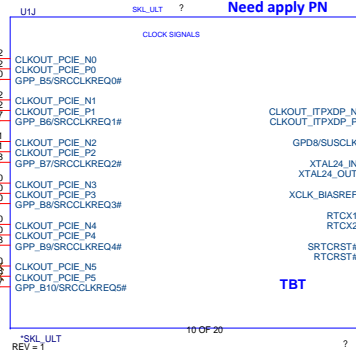
+1.0V_DEEP_SUS [9,15,16,39,40]
 +BAT_RTC [31]
 +1.8V_DEEP_SUS [5,9,15,39]
 +3V [2,4,10,12,15,21,25,27,29,30,32,33,35,41,45,46]
 +3VPCU [6,29,31,34,37,44]

0222 CQ
 Del CLK_PCIE_SSDN & CLK_PCIE_SSDP
 Change net name PCIE_CLKREQ_SSD# to PCIE_CLKREQ4#
 0311 CQ
 Add CLK_PCIE_SSDN & CLK_PCIE_SSDP for LG request
 Change net name PCIE_CLKREQ1# to PCIE_CLKREQ_SSD#

CLK_REQ/Strap Pin(CLG)

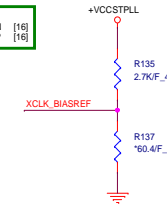


VGA
 [19] CLK_VGA_N
 [19] CLK_VGA_P
 [19] PCIE_CLKREQ_VGA#
SSD
 [32] CLK_PCIE_SSDN
 [32] CLK_PCIE_SSDP
 [32] PCIE_CLKREQ_SSD#
WLAN
 [31] CLK_PCIE_WLAN#
 [31] CLK_PCIE_WLANP
 [31] PCIE_CLKREQ_WLAN#
LAN
 [33] CLK_PCIE_LAN#
 [33] CLK_PCIE_LANP
 [33] PCIE_CLKREQ_LAN#
Cardreader
 [30] CLK_PCIE_CRN
 [30] CLK_PCIE_CRP
 [30] PCIE_CLKREQ_CR#
 0311 CQ
 Add CLK_PCIE_CRN & CLK_PCIE_CRP
 Change net name PCIE_CLKREQ4# to PCIE_CLKREQ_CR#

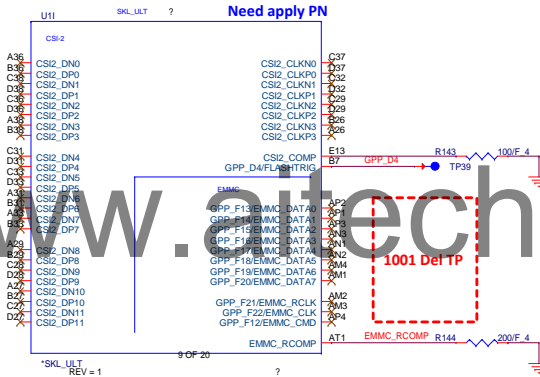


0305 CQ
 Change net name
 CK_XDP_N_R to CK_XDP_N
 CK_XDP_P_R to CK_XDP_P
 0307 CQ
 Add 0 ohm contact to page16 xDP
 XDP_N & XDP_P
 Del TP

1027 modify for easy layout

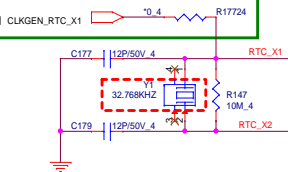


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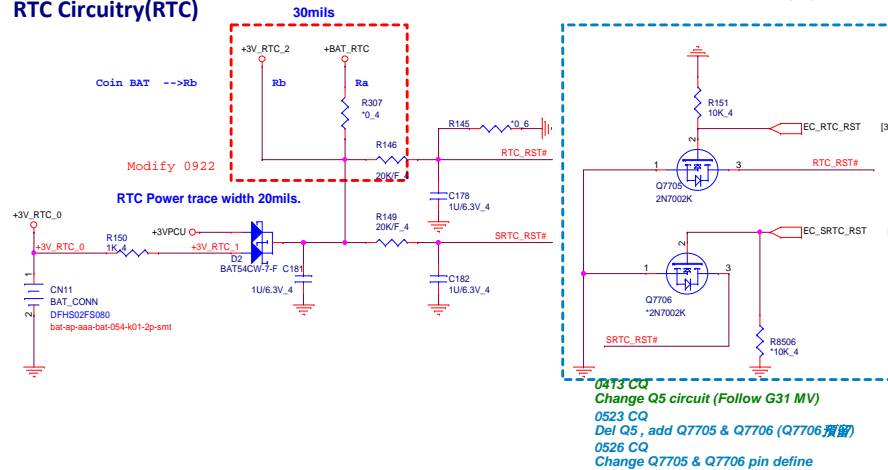


RTC Clock 32.768KHz

0301 CQ
 Add GCLK XTALIN (CLKGEN_RTC_X1) & 0ohm

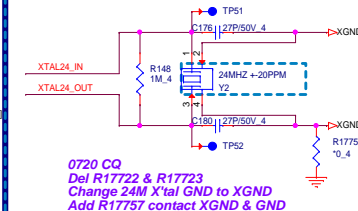


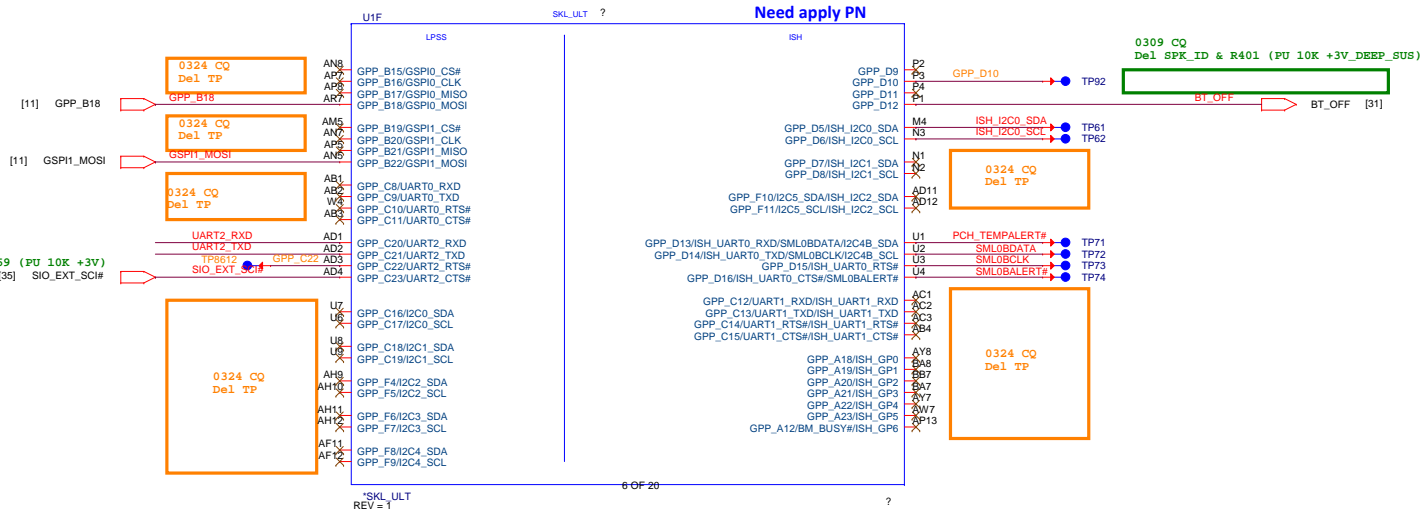
RTC Circuitry(RTC)



External Crystal

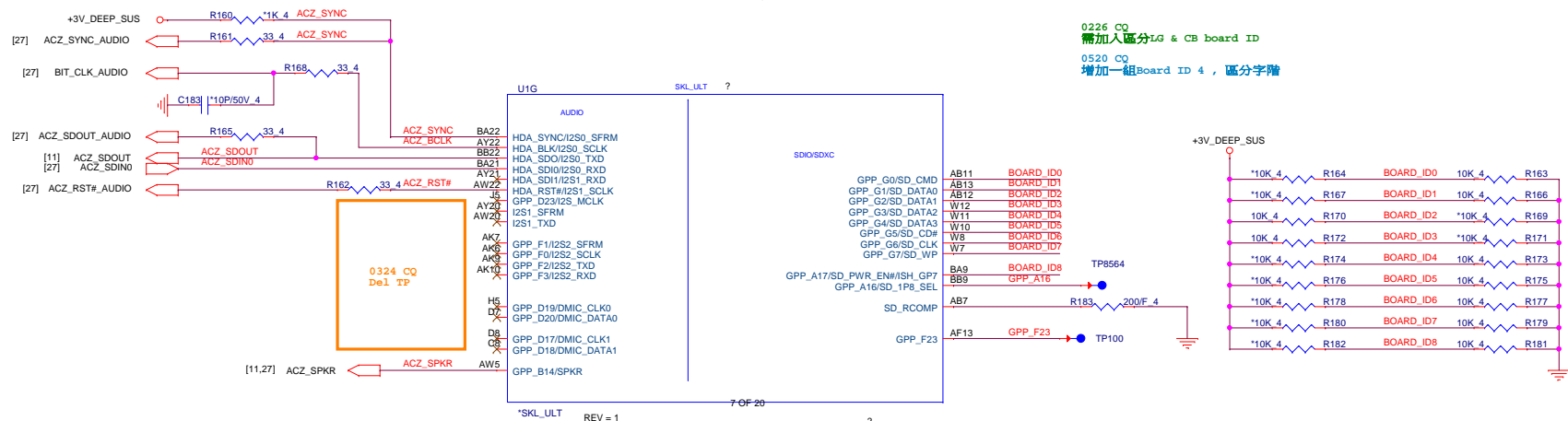
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



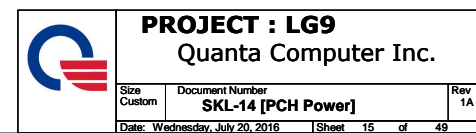


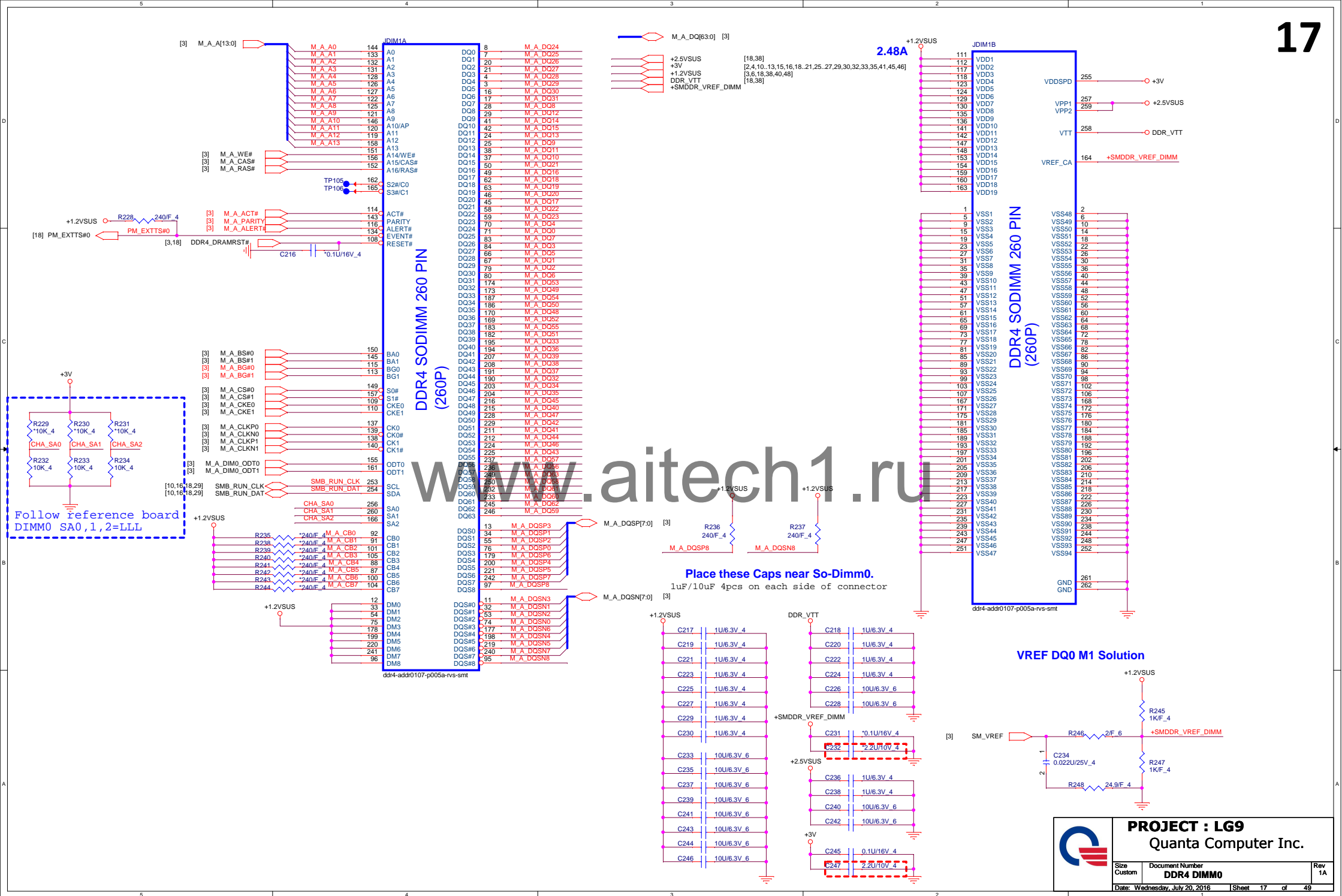
HDA Bus(CLG)

Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4	BOARD_ID5	BOARD_ID6	BOARD_ID7	BOARD_ID8
	GPP_G0	GPP_G1	GPP_G2	GPP_G3	GPP_G4	GPP_G5	GPP_G6	GPP_G7	GPP_G8
	LG9 : 0 LG9A : 1	LG : 0 CB : 1	N16V : 0 N16S : 1	UMA : 0 dGPU : 1	LG9 : 0 LG9A : 1	No Define	No Define	No Define	No Define
LG9 + UMA	0	0	0	0	0	0	0	0	0
LG9 + dGPU + N16S-GTR	0	0	1	1	0	0	0	0	0
LG9 + dGPU + N16V-GMR1	0	0	0	1	0	0	0	0	0
LG9A + UMA	1	1	0	0	1	0	0	0	0
LG9A + dGPU + N16S-GTR	1	1	1	1	1	0	0	0	0
LG9A + dGPU + N16V-GMR1	1	1	0	1	1	0	0	0	0

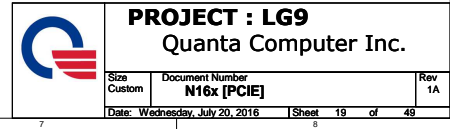


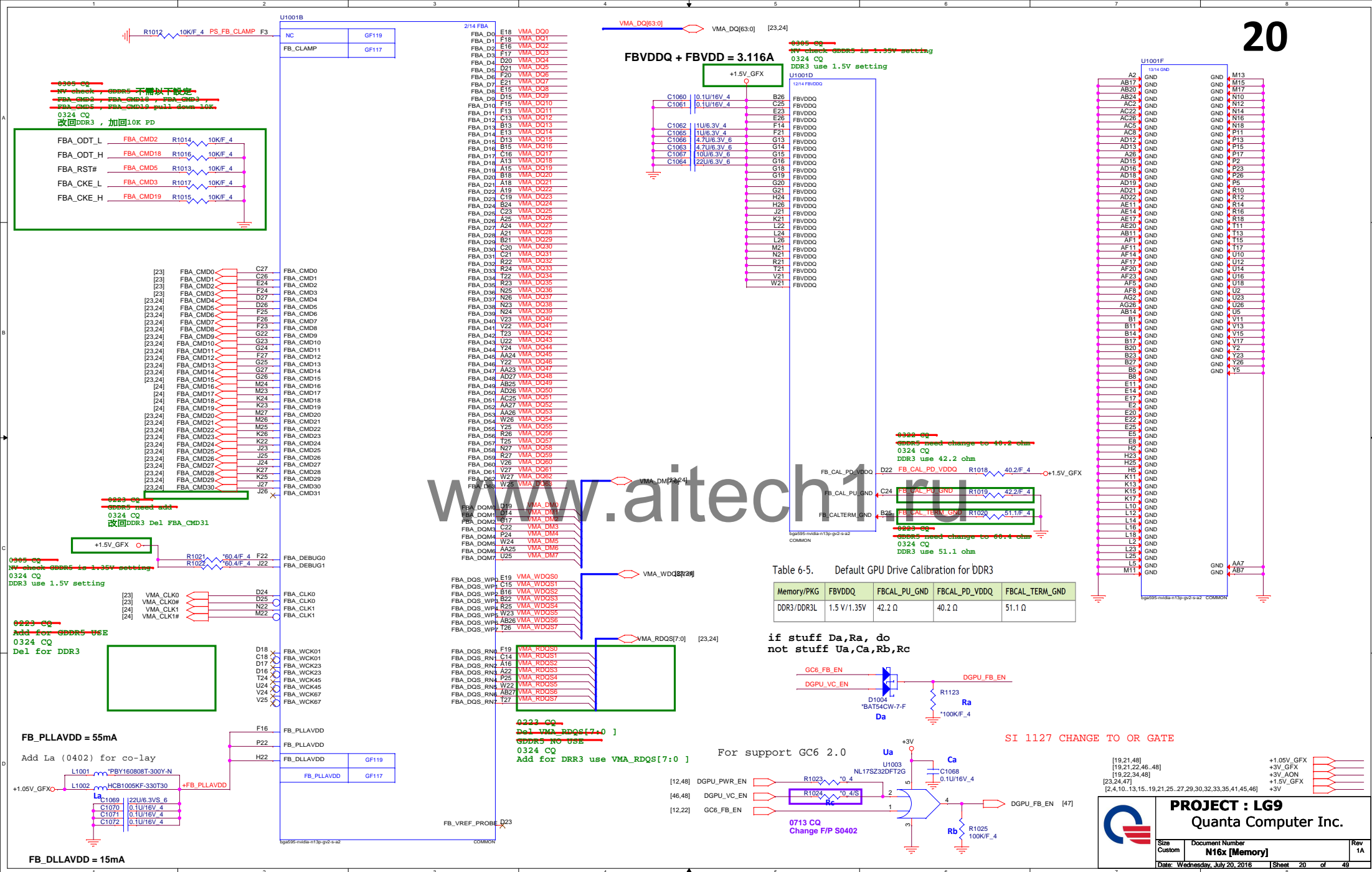
Size Custom	Document Number SKL-13 [GPIO]	Rev 1A
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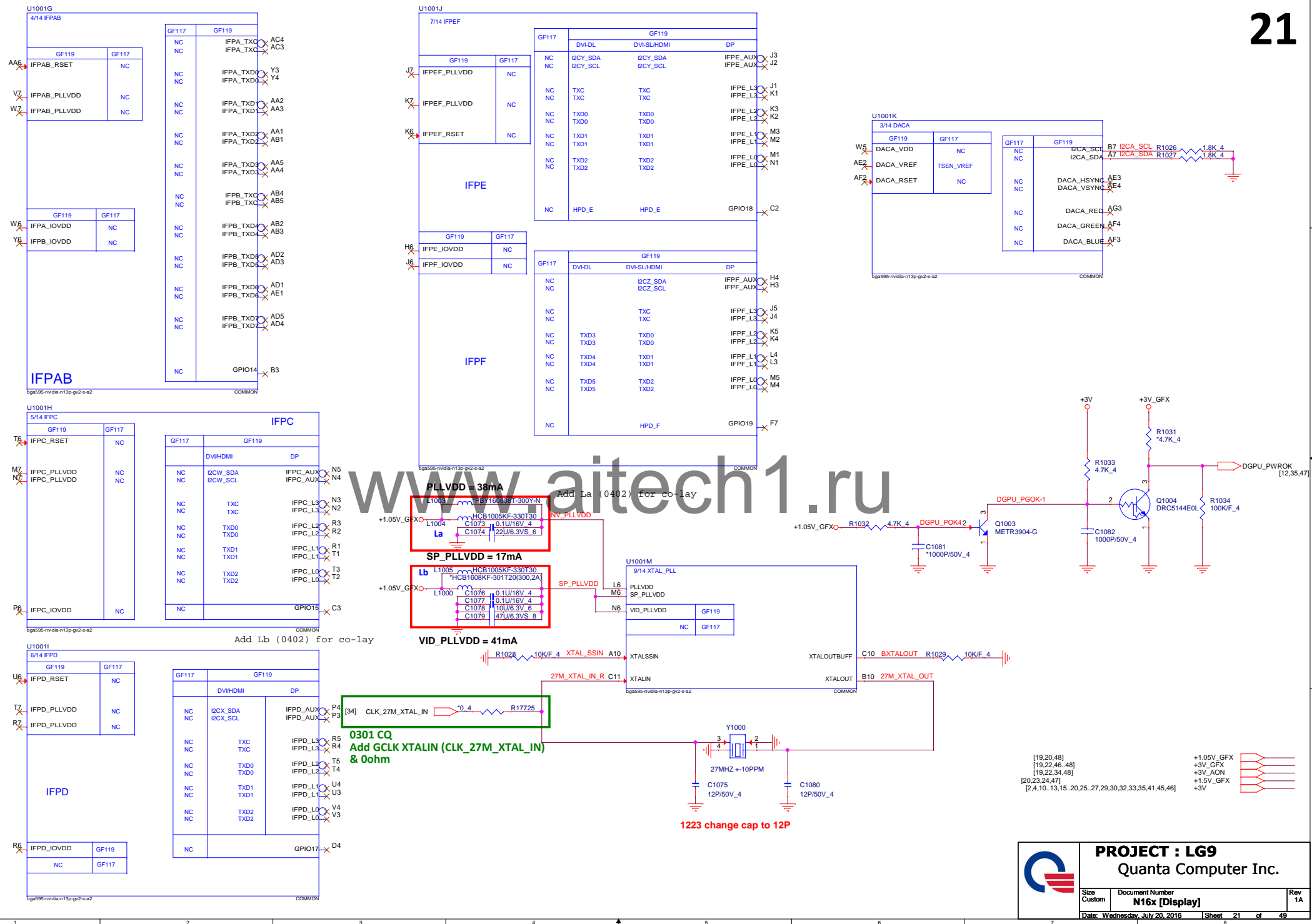










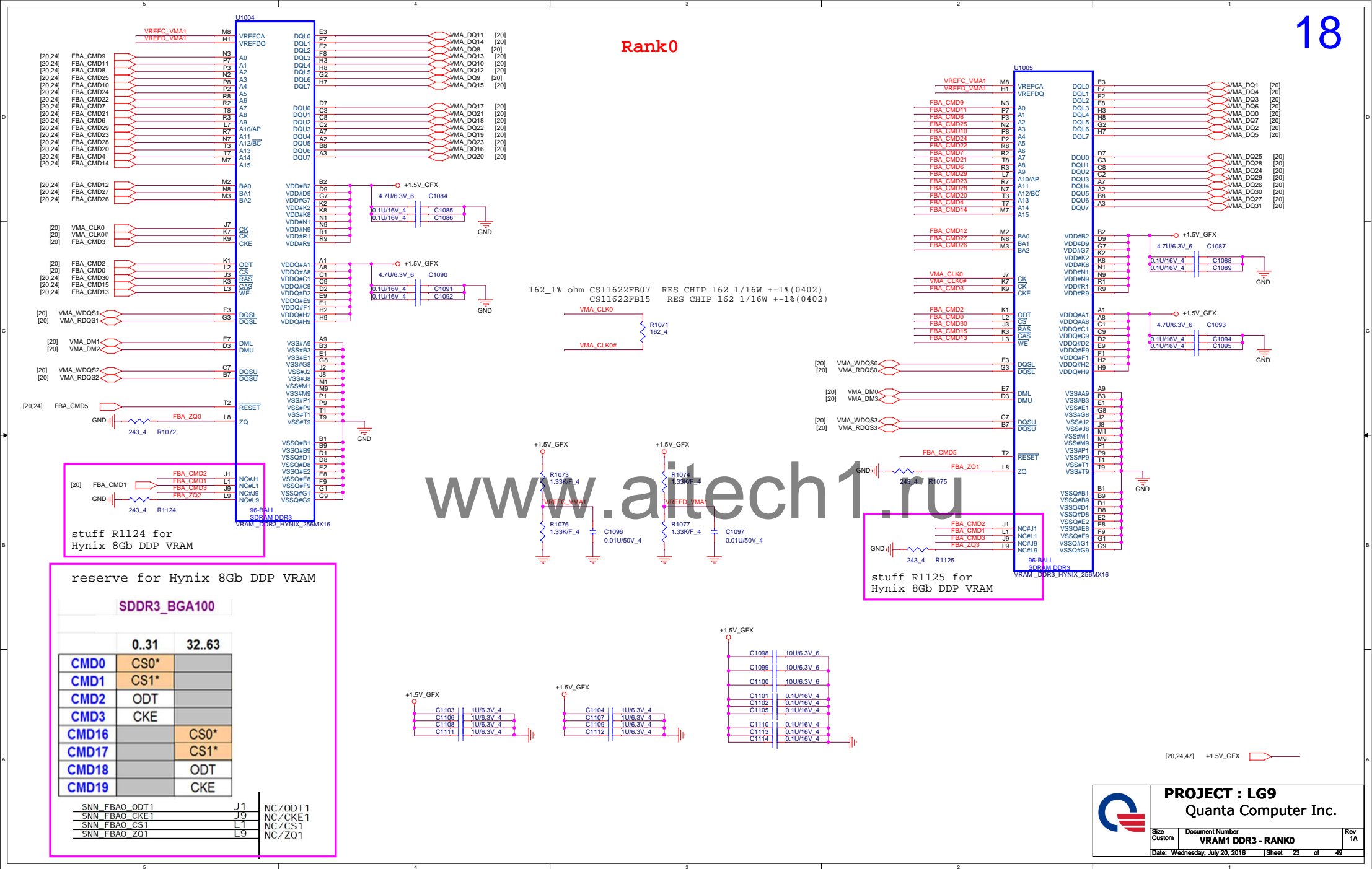


--	--	--	--

Memory	FBVDD/	Memory			Manufacturer	Die
--------	--------	--------	--	--	--------------	-----

+3V_GFX [19,21,46,48]

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
-----------------	---------------------	------------------

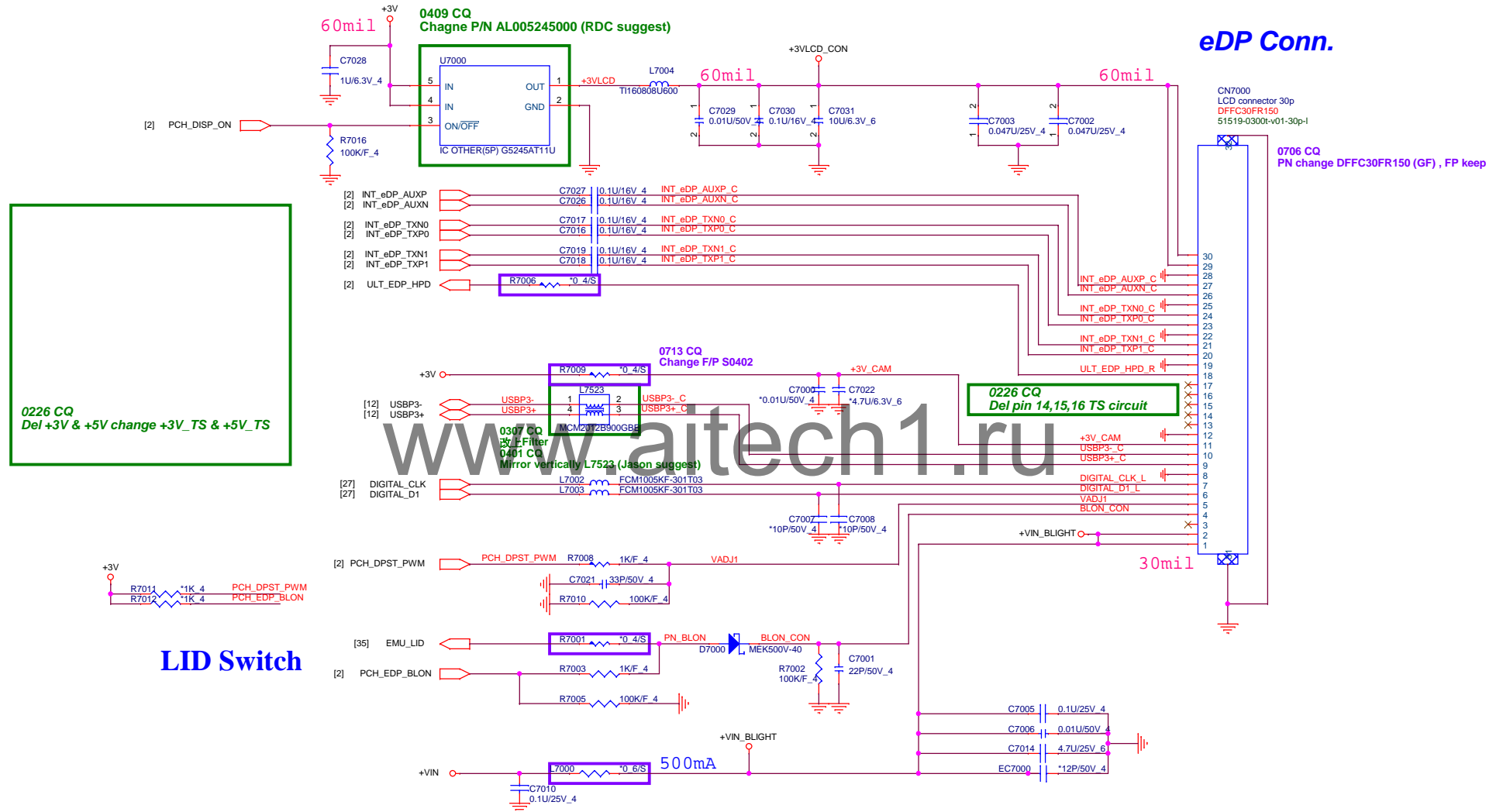




PROJECT : LG9
Quanta Computer Inc.

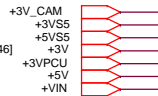
Size Custom	Document Number VRAM2 DDR3 - RANK0	Rev 1A
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0219 CQ
Re-draw & Compare OK



LID Switch

[4,10,15,16,27,31,32,35,37..40,44,45,48]
[4,26,32,37..43,45..48]
[2,4,10..13,15..21,26,27,29,30,32,33,35,41,45,46]
[6,13,29,31,34..37,44]
[26,27,29,45]
[36..39,41..44,46,47,49]

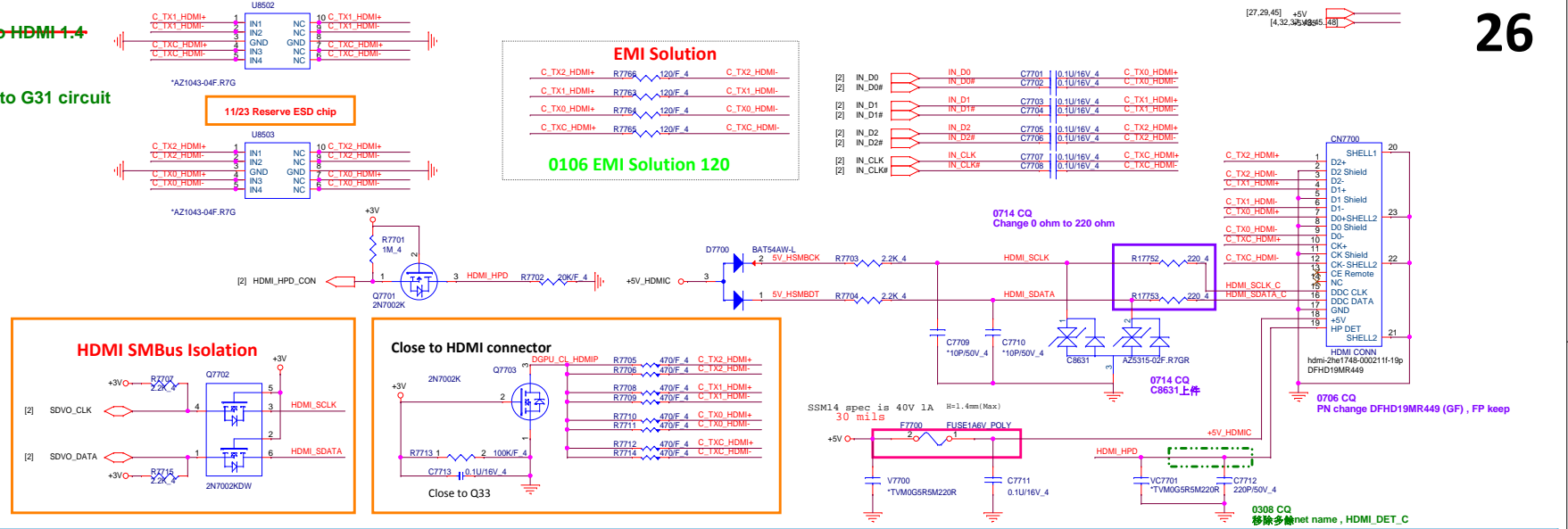


PROJECT : LG9
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Size Custom	Document Number eDP	Rev 1A
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~~0301 CQ~~
~~Del HDMI 2.0 circuit , Change to HDMI 1.4~~
~~Use TWL circuit~~

0305 CQ
 Del TWL HDMI circuit , change to G31 circuit

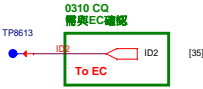
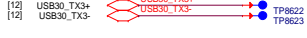
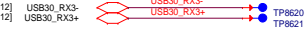
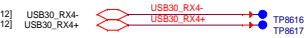
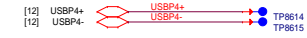


USB 2.0/3.0 Combo

USB 3.0

0305 CQ
 USB3 cricuit Change Page 28 to 26



PROJECT : LG9
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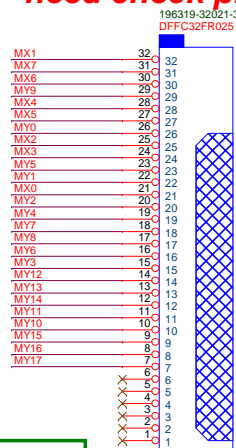
0412 CQ
刪除TypeC線路，保留USB & ID2 線段

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KEYBOARD Con.

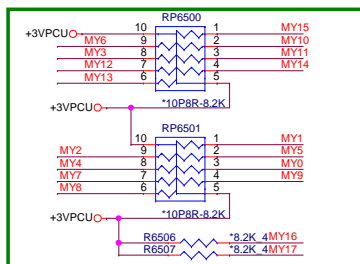
[35] MY[0..17]  MY[0..17]
[35] MX[0..7]  MX[0..7]

need check pin define

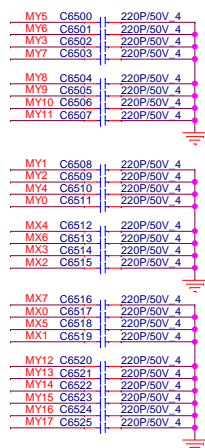


0307 CQ
Del CAPSLED# & MUTE_LED_CNTL cricuit
(Use TWL KB)
0411 Dennis
Swap KB Pin define for ME request

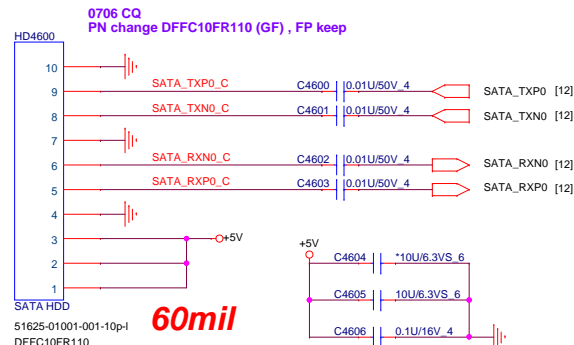
KEYBOARD PULL-UP



0406 CQ
Swap pin for layout
0412 CQ
Swap pin for layout again



HDD



60mil

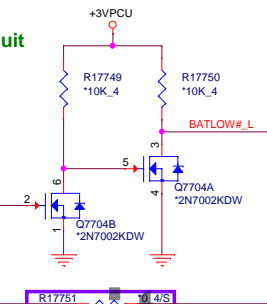
[2,4,10,13,15,21,25,27,30,32,33,35,41,45,46]
[6,13,31,34,37,44]
[26,27,45]
[45]
[25]
[25,36,39,41,44,46,47,49]

+3V
+3VPCU
+5V
+3VSUS
+3V_CAM
+VIN

0307 CQ
刪除SATA LED雙色燈 circuit

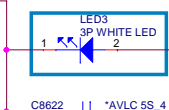
0226 CQ
Del IR CAM circuit

0316 CQ
Add LED circuit
(小板移植)

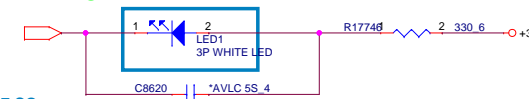


0508 CQ
Change LED1, LED2, LED3 F/P ledltw-110uc5-3p

BAT LED

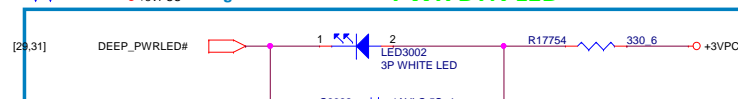


SATA LED

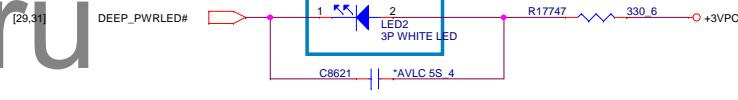


0517 CQ
Add PWR BTN LED
0518 CQ
Change LED3002 P/N & FP

PWR BTN LED

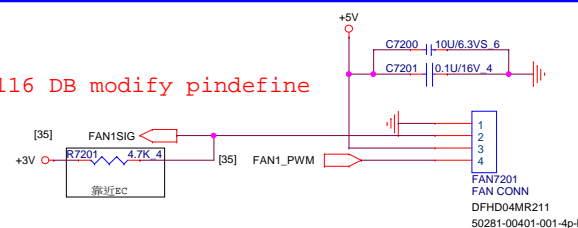


PWR LED



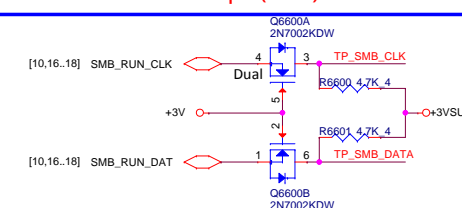
FAN

1116 DB modify pindefine

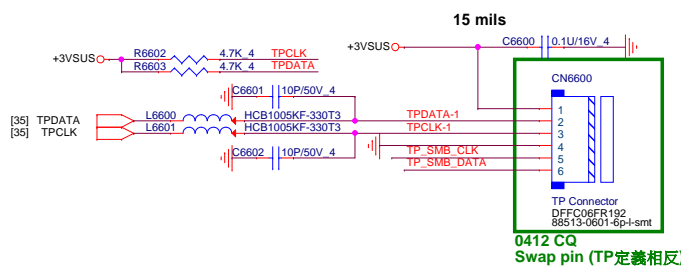


FAN1_PWM C7202 *220P/50V_4
FAN1SIG C7203 *220P/50V_4

0330 CQ
PN DFHD04MR211
FP 50281-00401-001-4p-I (0408)



Touch Pad Connector



0412 CQ
Swap pin (TP定義相反)

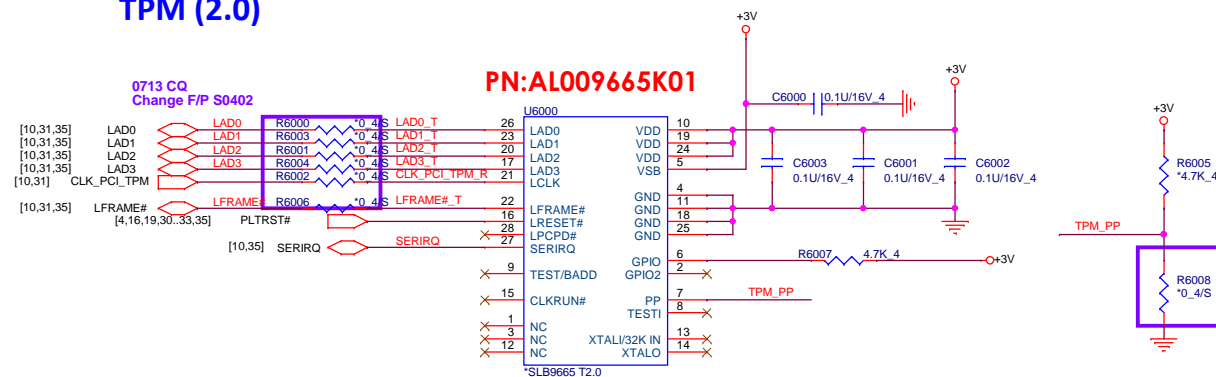


PROJECT : LG9
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Size	Document Number	Rev
Custom	HDD/ TP / KB / FAN / LED	1A

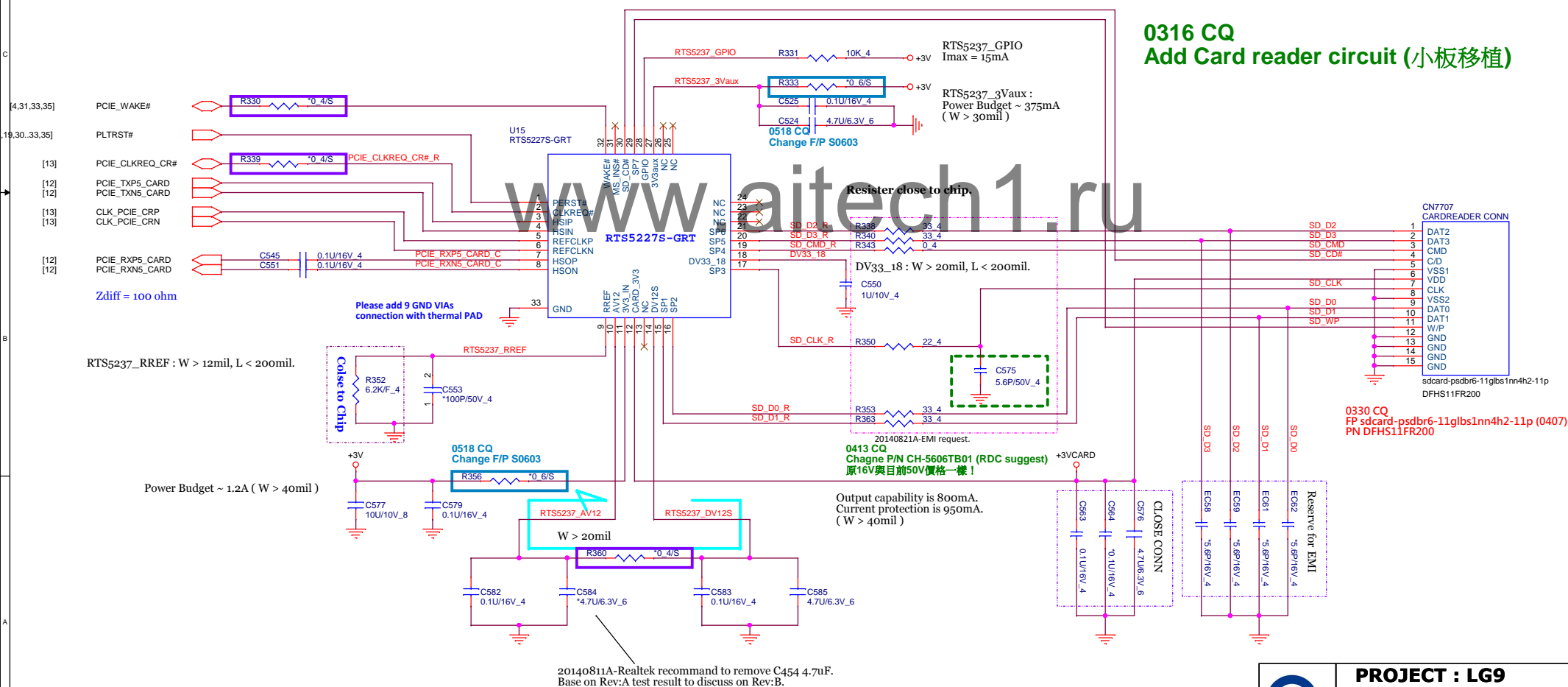
Date: Wednesday, July 20, 2016 Sheet 29 of 49

TPM (2.0)



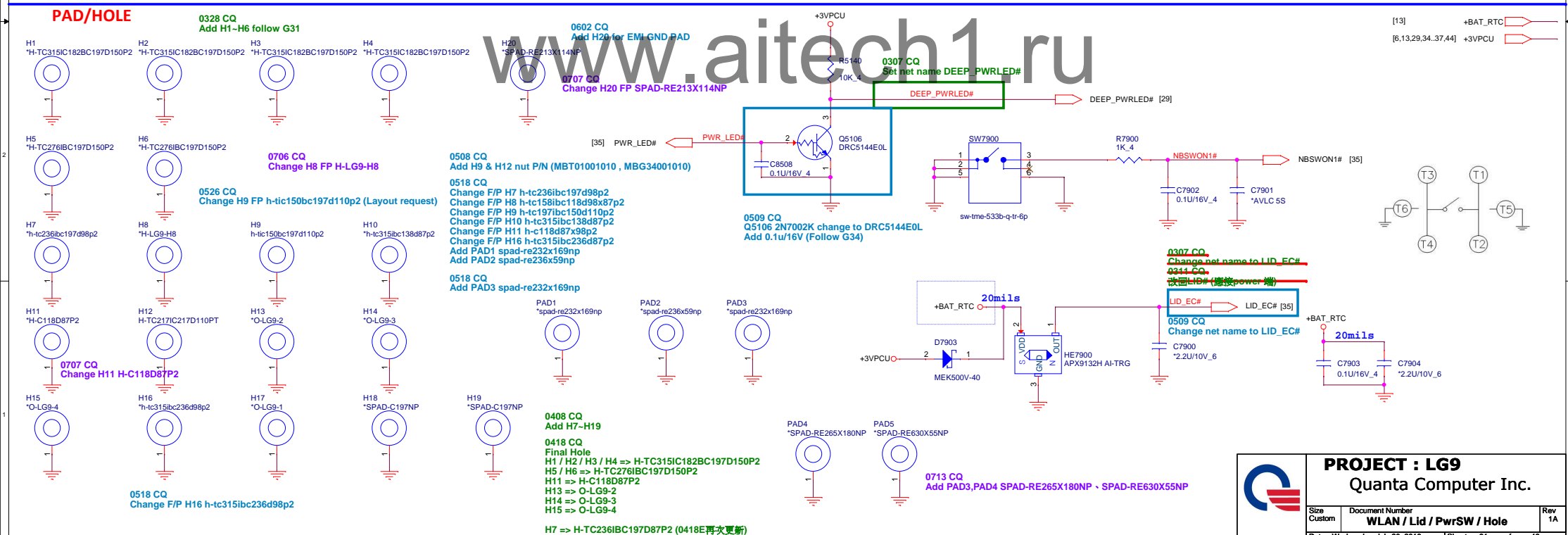
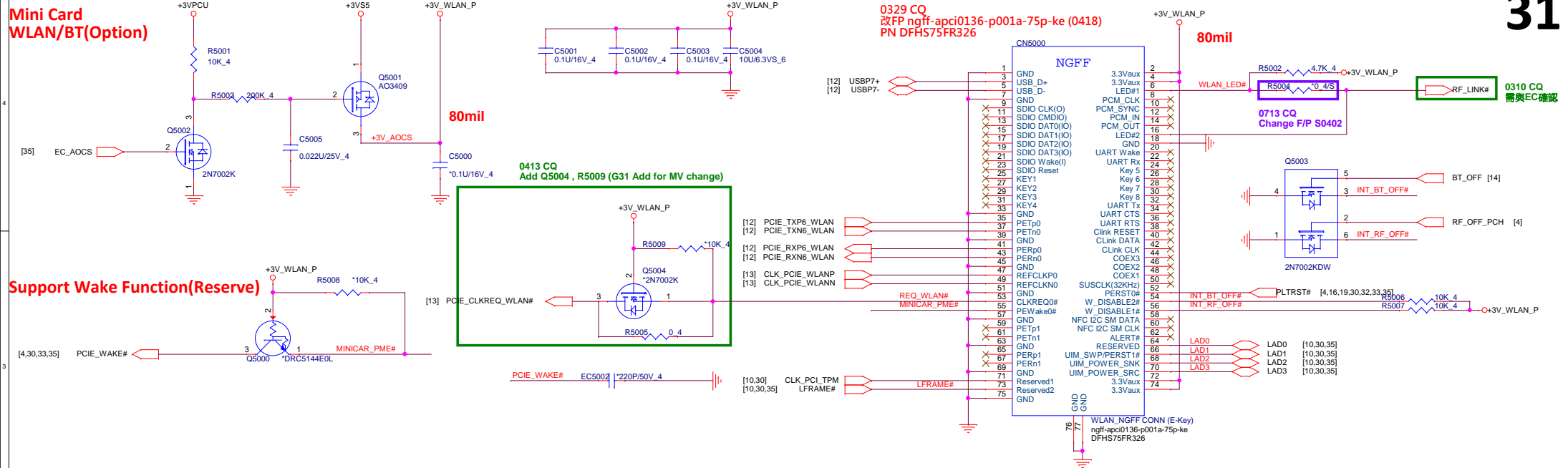
0307 CQ

Del G-sensor circuit



PROJECT : LG9
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0226 CQ
Del PCIe port11
0311 CQ
Add PCIe SSD function for LG request

0315 CQ
Remove 0 ohm & Net name
R17739 & R17740
PCIe_RXN11_SSD_C & PCIe_RXP11_SSD_C

0525 CQ
Add PCIe SSD to 4ch

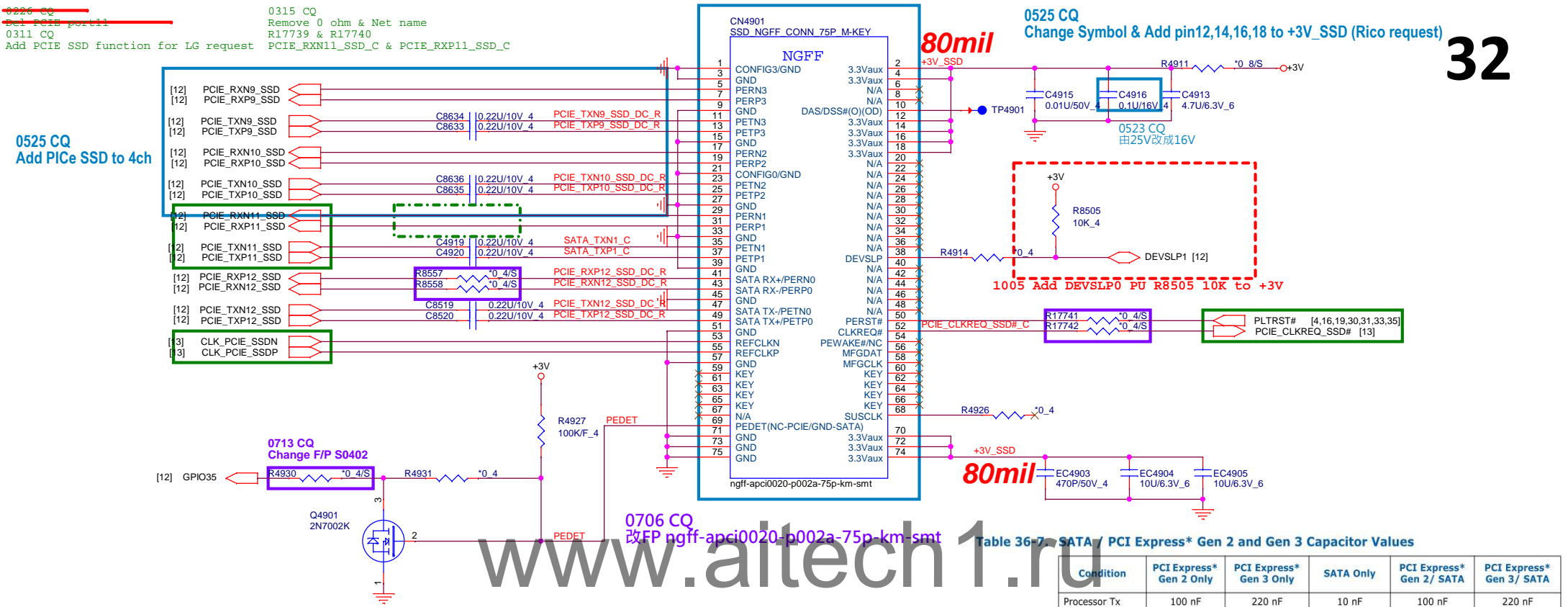


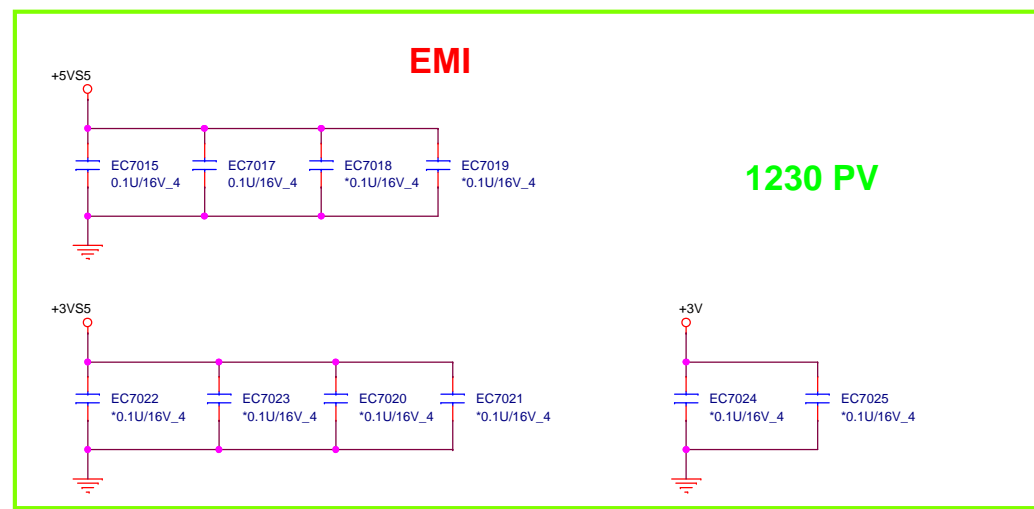
Table 36-7: SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values


Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

[2,4,10,13,15,21,25,27,29,30,33,35,41,45,46] +3V





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Size B	Document Number NGFF (PCIe/SATA)	Rev 1A
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9. Power Sequence

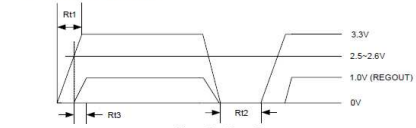
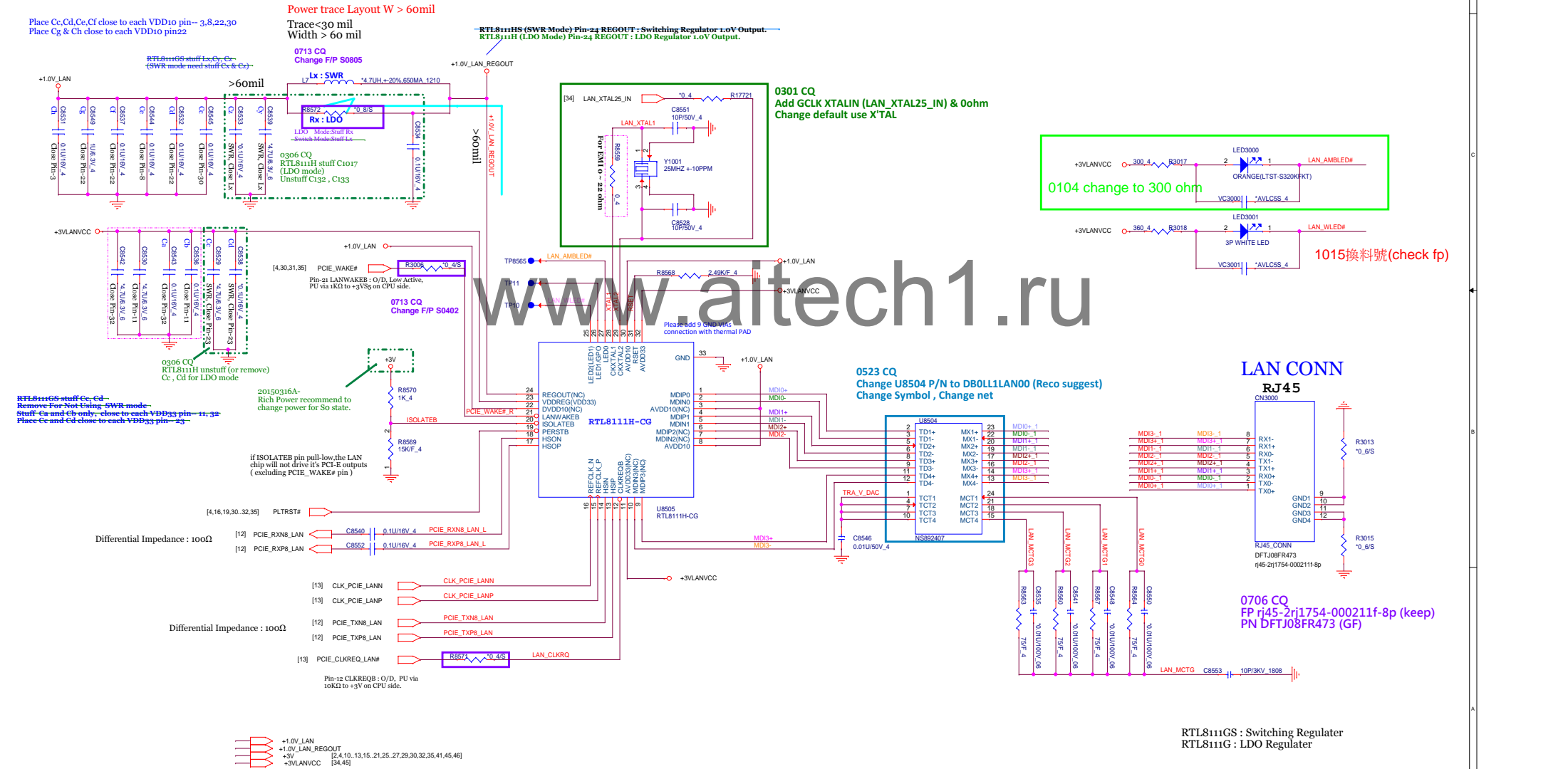


Table 16. Power Sequence Parameter

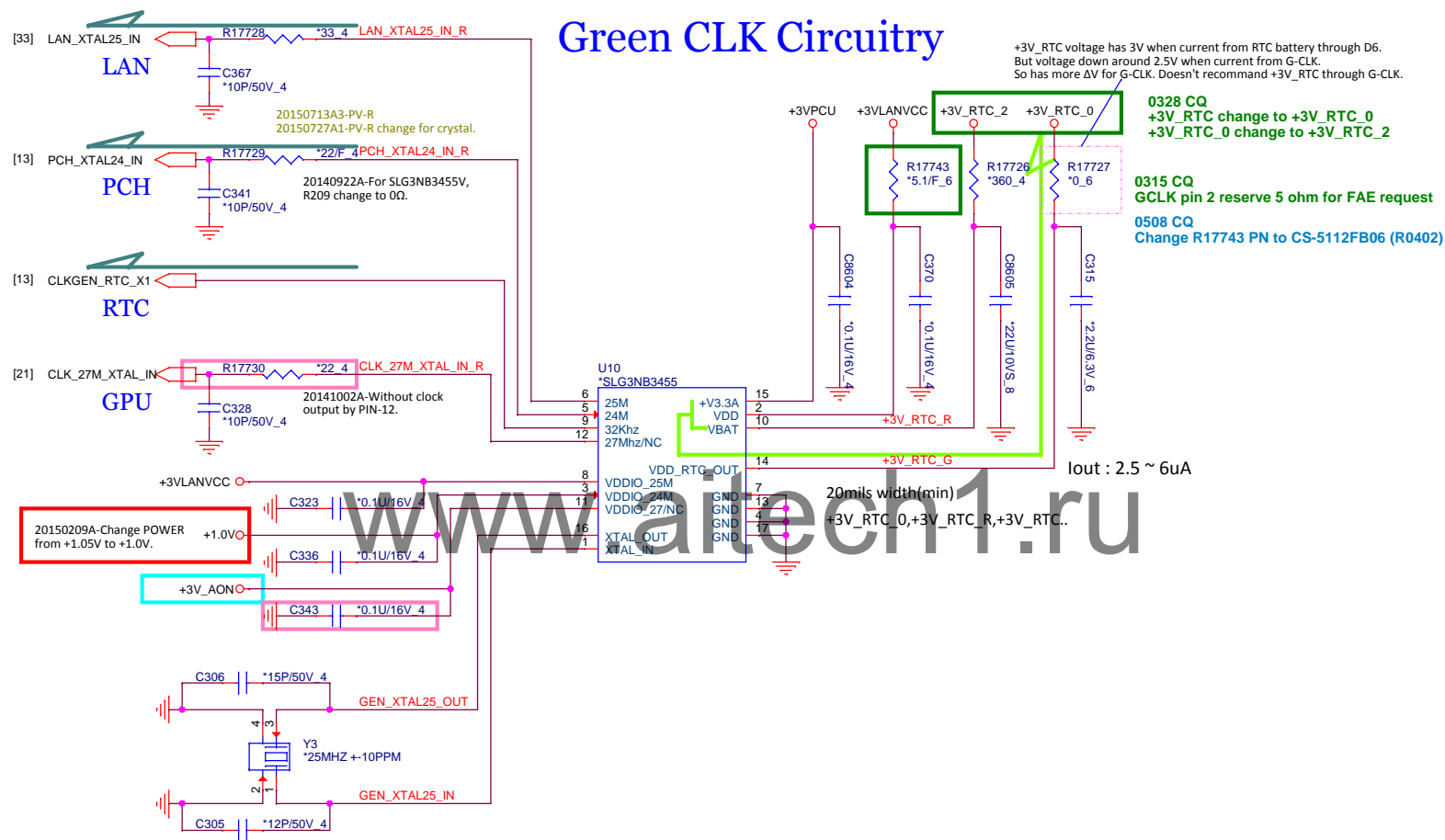
Symbol	Description	Min	Typical	Max	Units
R1	3.3V Rise Time	0.5	-	100	ms
R2	3.3V Off Time	50	-	-	ms
R3	1.0V (REGOUT) Settle Time	-	-	15	ms


Note: See the following section for power sequence requirements.

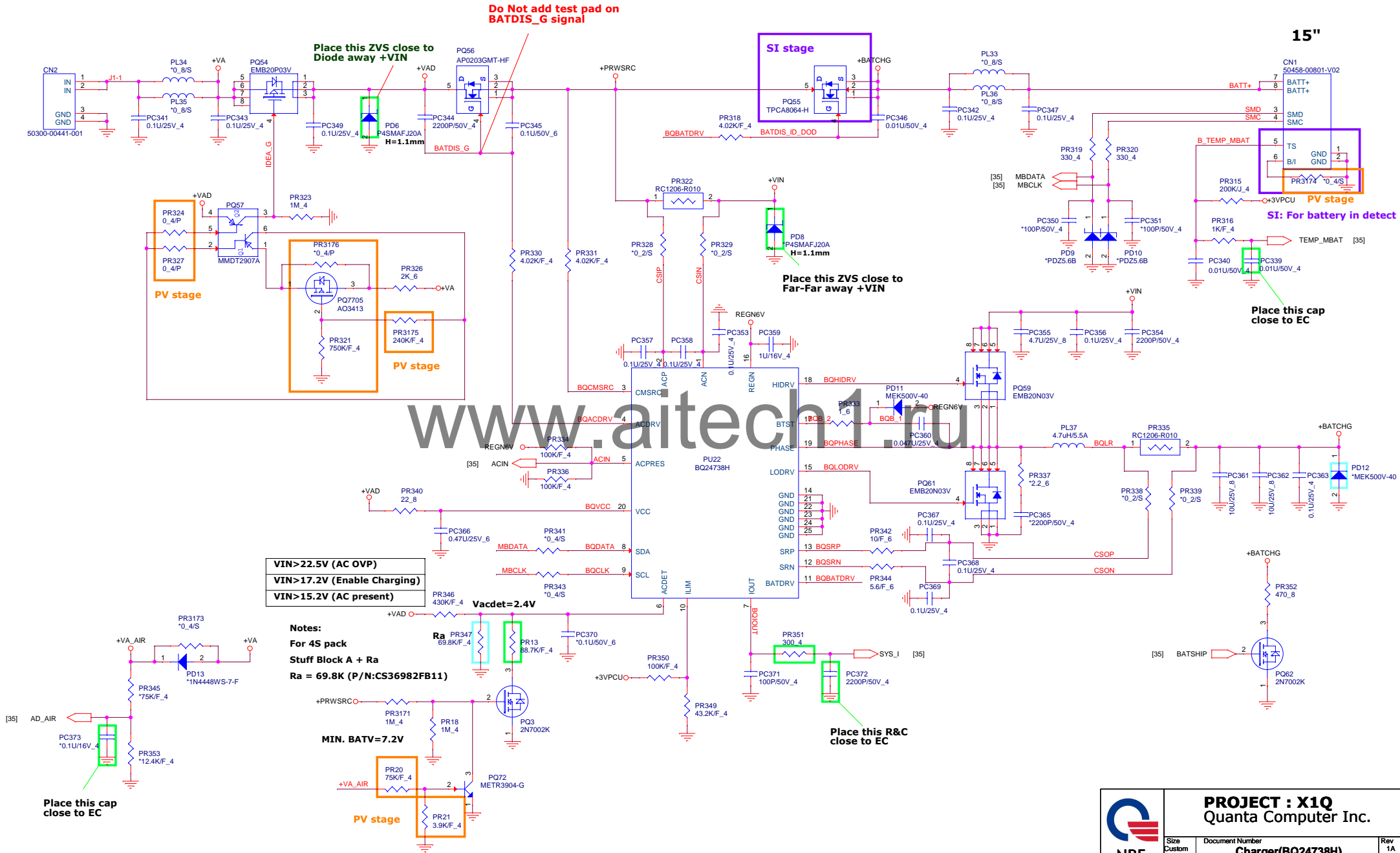


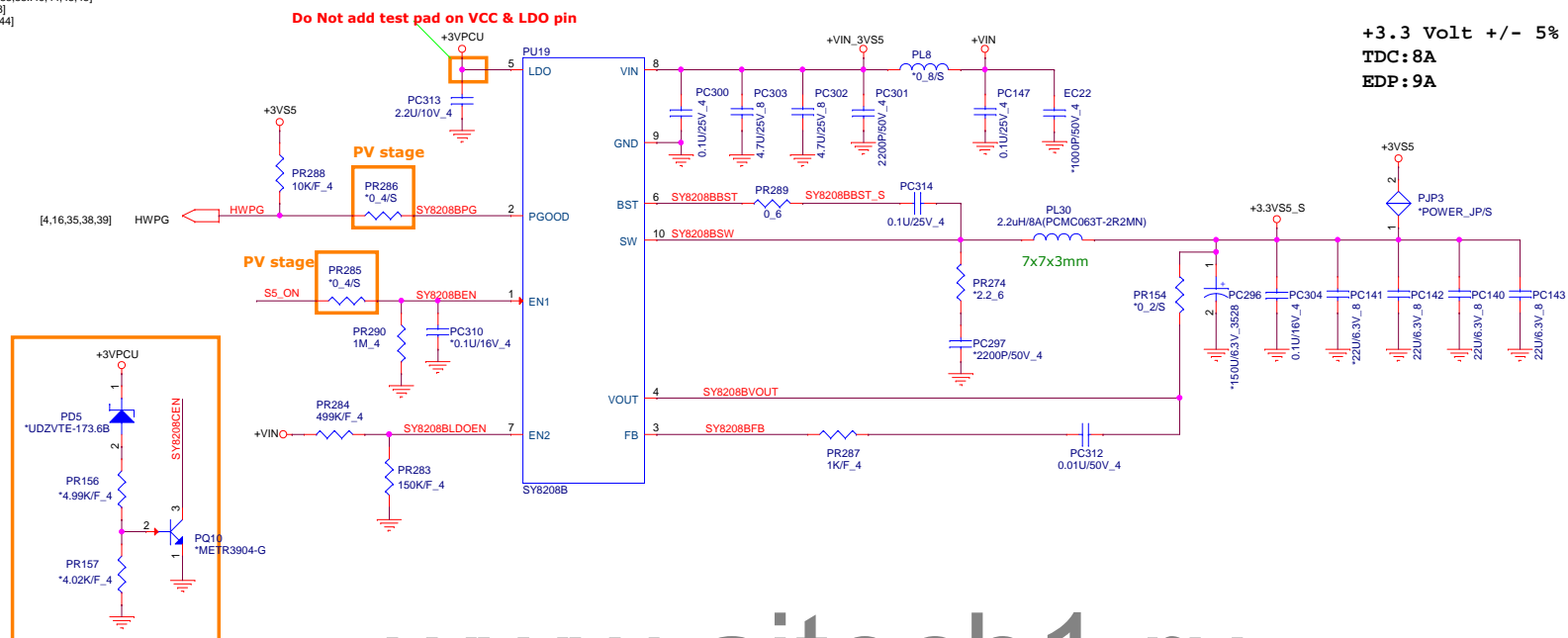
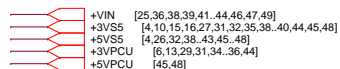
0226 CQ Use TWL GCLK circuitry

32

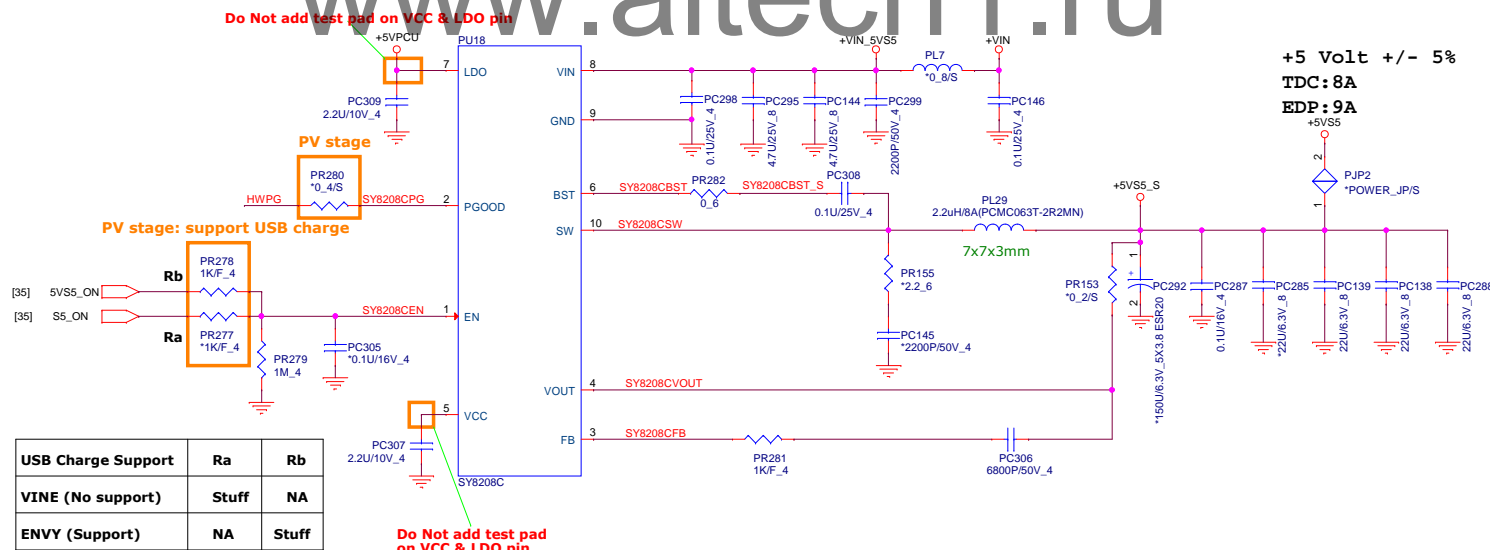


 PROJECT : LG9 Quanta Computer Inc.		
Size B	Document Number GCLK-SLG3NB3455	Rev 1A
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+3.3 Volt +/- 5%
TDC:8A
EDP:9A

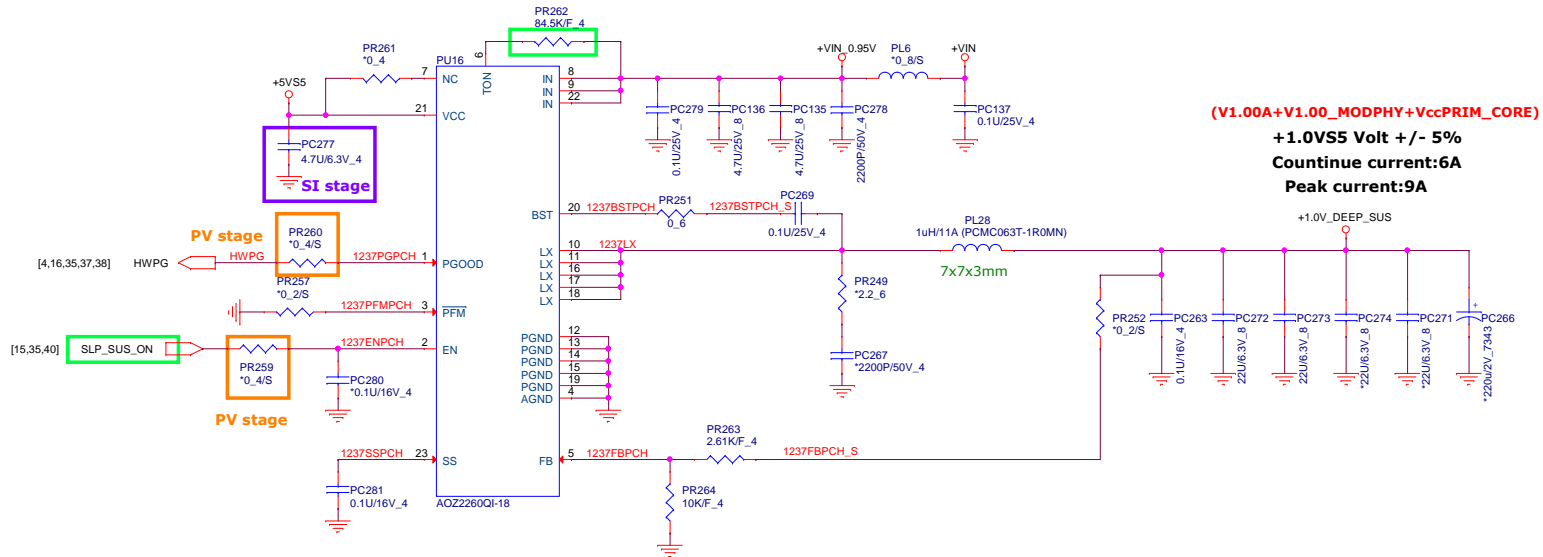


+5 Volt +/- 5%
TDC:8A
EDP:9A

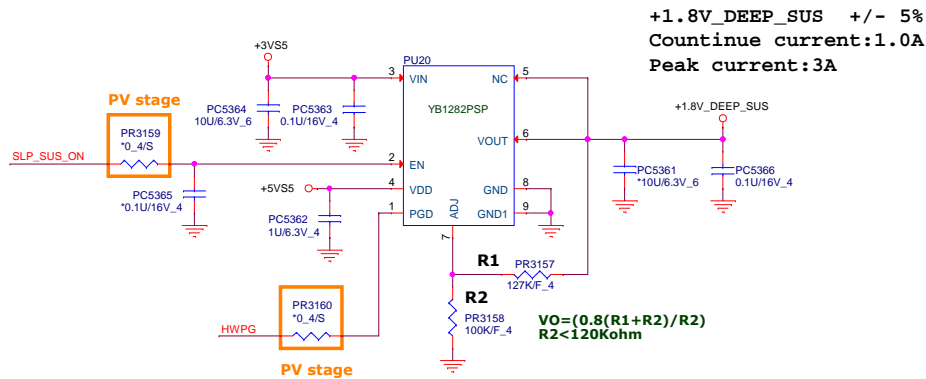
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff



+VIN [25,36,38,41,44,46,47,49]
 +3VS5 [4,10,15,16,27,31,32,35,37,38,40,44,45,48]
 +5VS5 [4,26,32,37,38,40,43,45,48]
 +1.0V_DEEP_SUS [9,15,16,40]
 +1.8V_DEEP_SUS [5,9,15]



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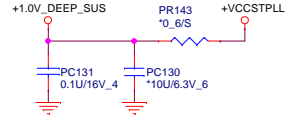


+1.0V	[2,4,6,16,34,35]
+3VSS	[4,10,15,16,27,31,32,35,37,39,44,45,48]
+5VSS	[4,26,32,37,39,41,43,45,48]
+VCCIO	[6,16]
+1.2VSUS	[3,6,17,18,38,48]
+VCCSTPLL	[2,4,6,9,13,41]
+1.0V_DEEP_SUS	[9,15,16,39]
+1.2V_VCCPLL_OC	[6]
MAINON	[26,35,38,40,45]

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

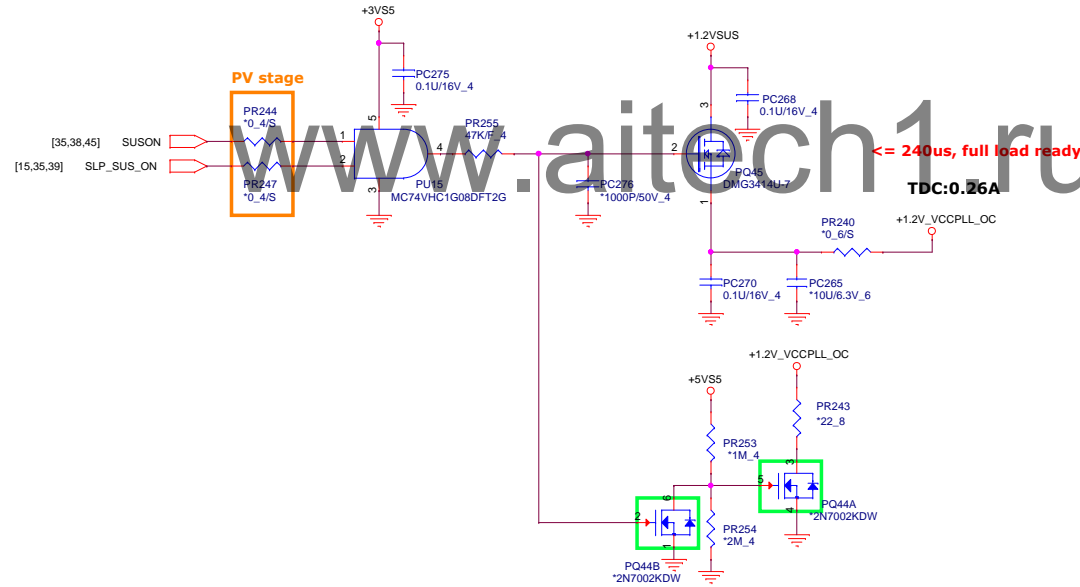
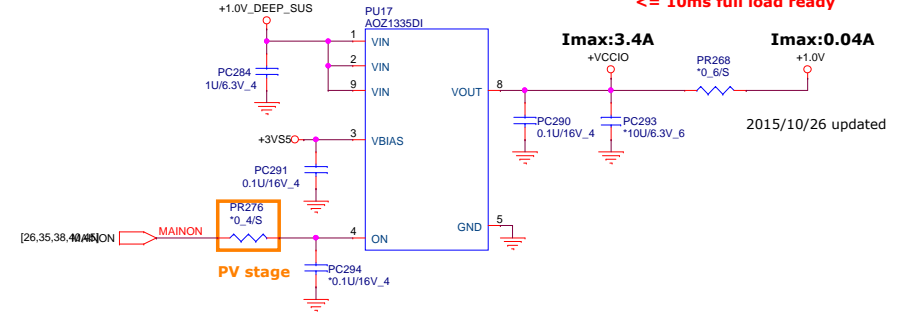
Imax:0.24A



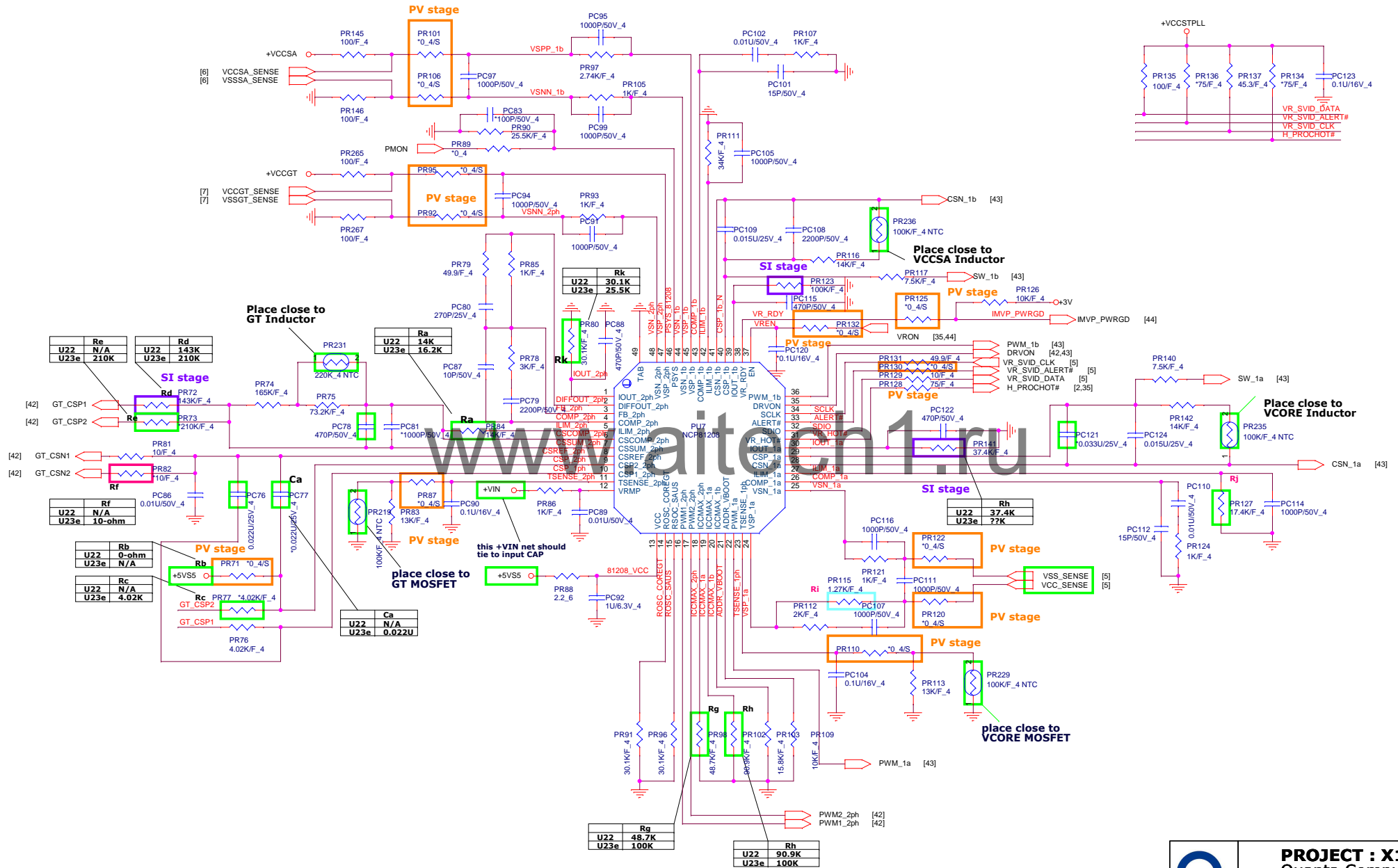
Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

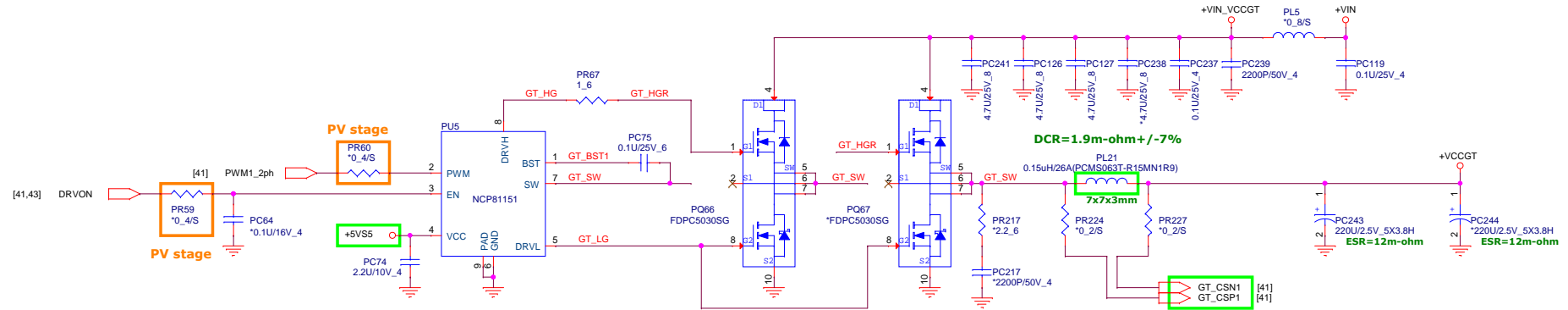
Imax:3.4A **Imax:0.04A**



	PROJECT : X1Q		
	Quanta Computer Inc.		
	Size Custom	Document Number +1.0V/+VCCSTPLL	Rev 1A
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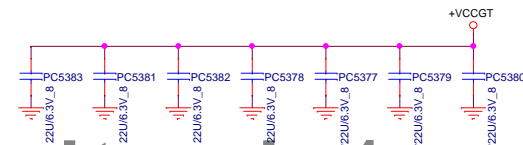


+5V [26,27,29,45]
 +VIN [25,36,39,41,43,44,46,47,49]
 +5VPCU [37,45,48]
 +VCCGT [7,41]



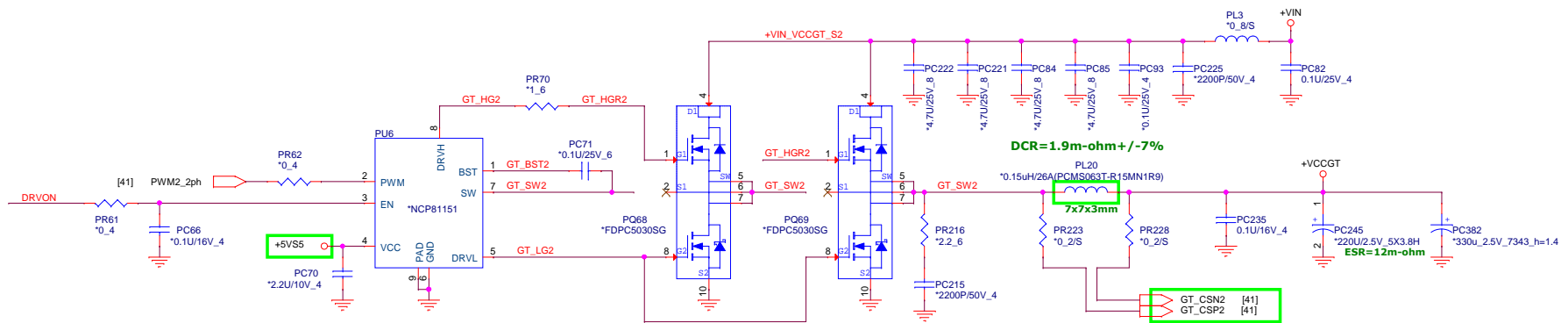
For U23e --> Add These Components

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+VCCGT

U-line 22 (15W)
 TDC:18A(22)
 Icc max:31A(22)
 L/L=3.1mV/A
 U-line 23e(28W)
 TDC:35A(23e)
 Icc max =64A(GT+GTx)
 L/L=2mV/A

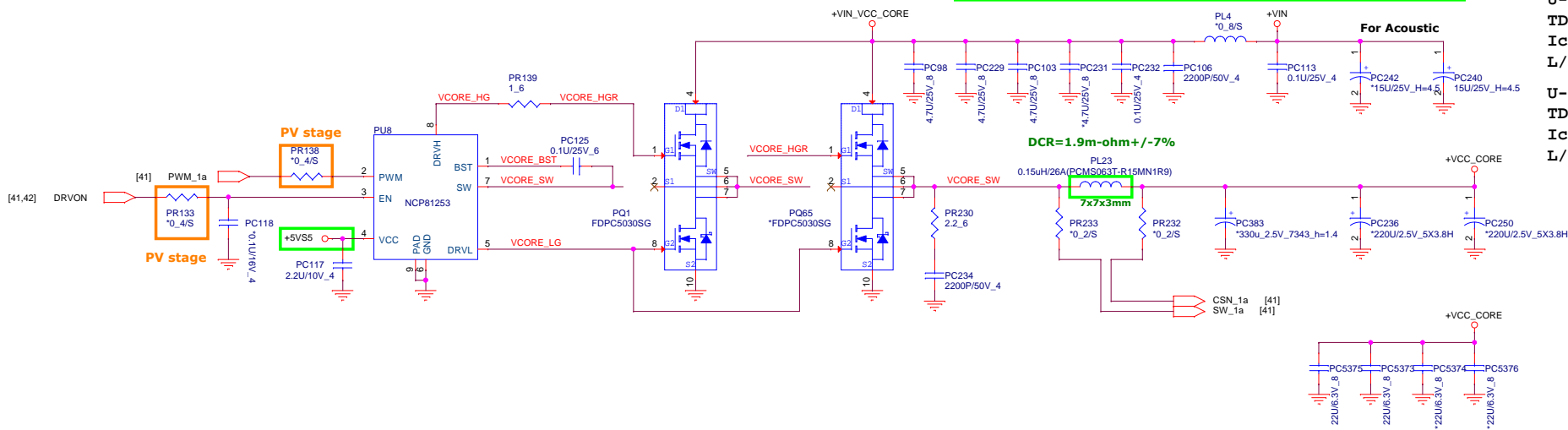


PROJECT : X1Q
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
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CPU CORE

+VIN [25,36,39,41,42,44,46,47,49]
+5VPCU [37,45,48]
+VCCSA [6,41]
+VCC_CORE [5]

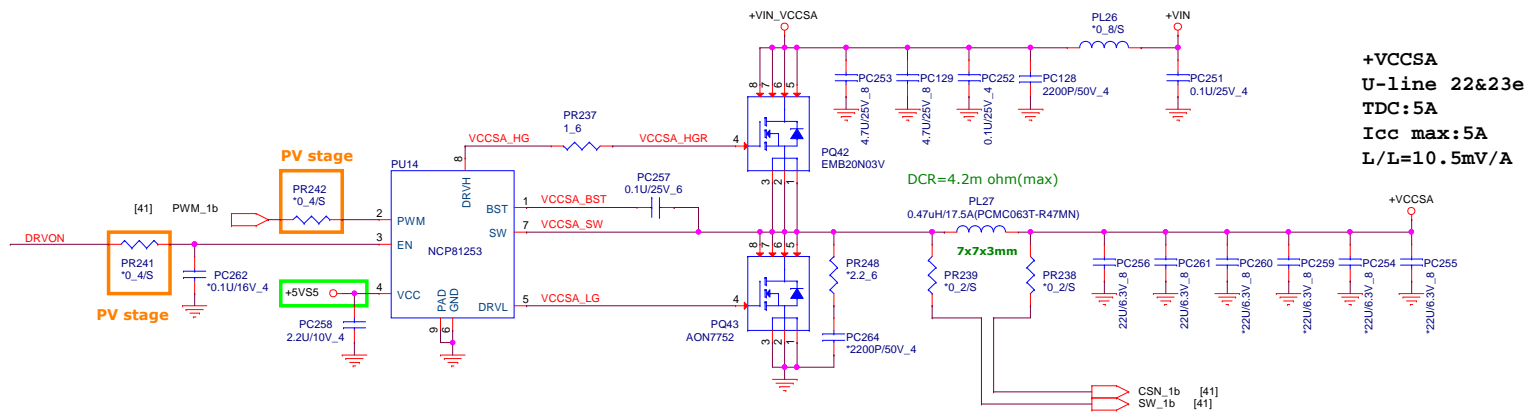


+VCC_CORE
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A
U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

43

VCCSA

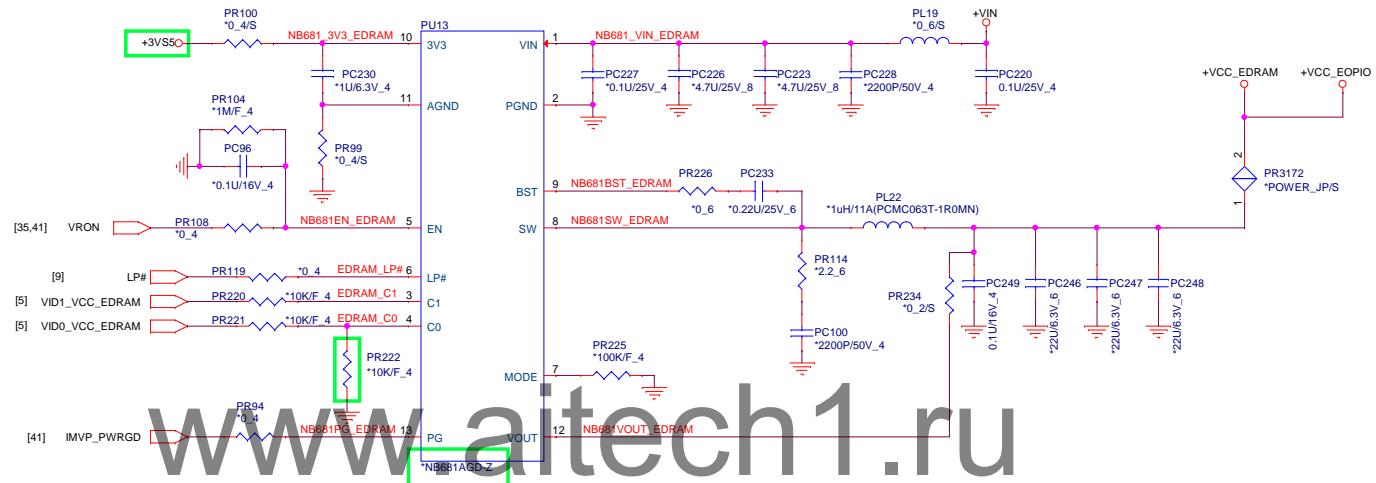
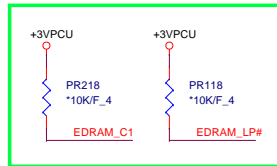
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+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

+VIN [25,36,39,41,43,46,47,49]
 +3VPCU [6,13,29,31,34,37]
 +VCC_EOPIO [5]
 +VCC_EDRAM [5]
 +3VS5 [4,10,15,16,27,31,32,35,37,40,45,48]

+VCC_EDRAM +/- 5%
 Countinue current:4.5A
 Peak current:6A



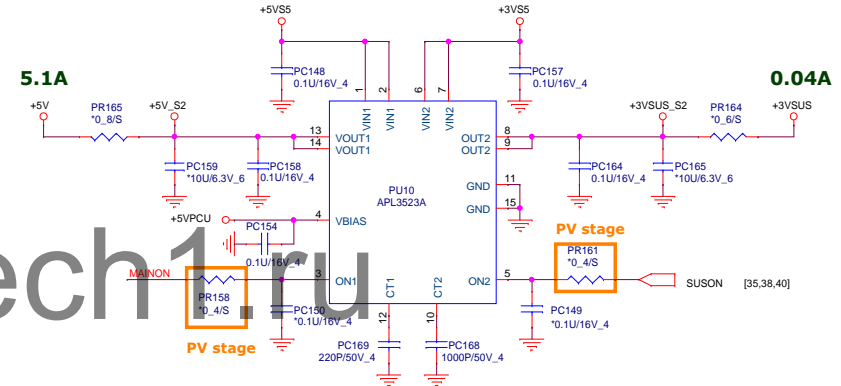
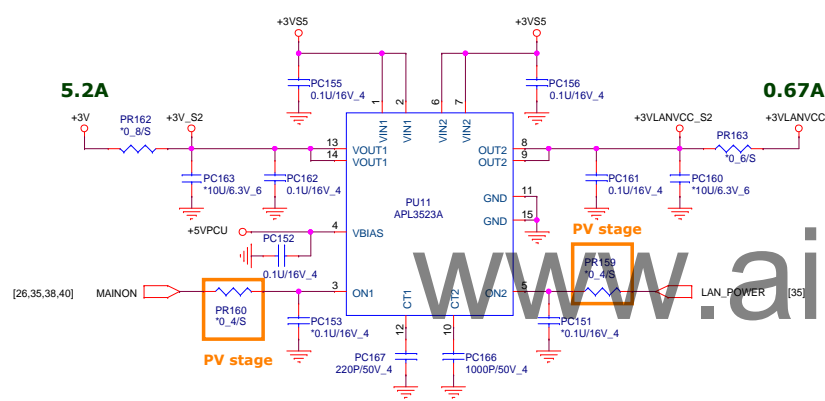
VCC_EDRAM

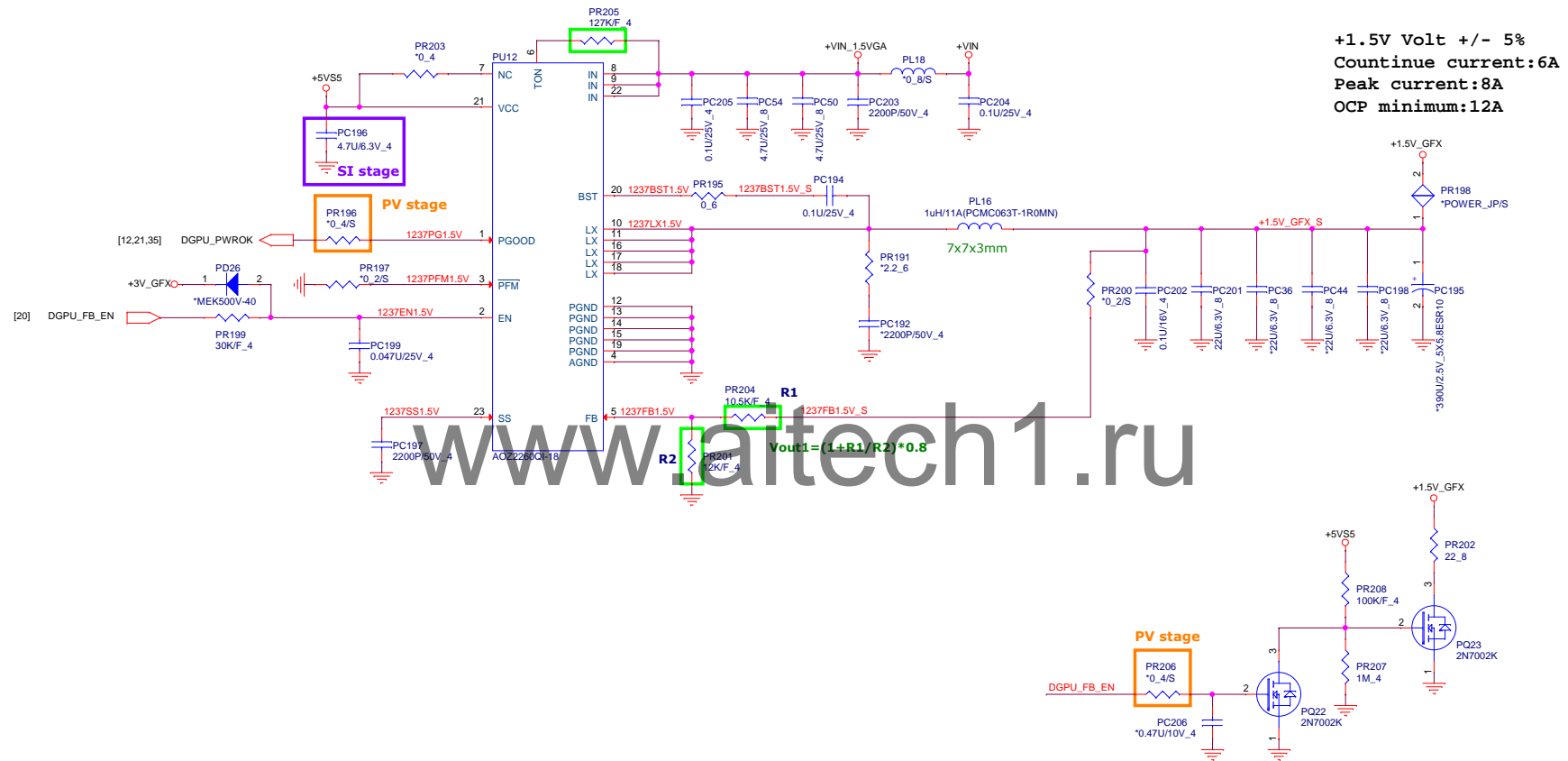
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

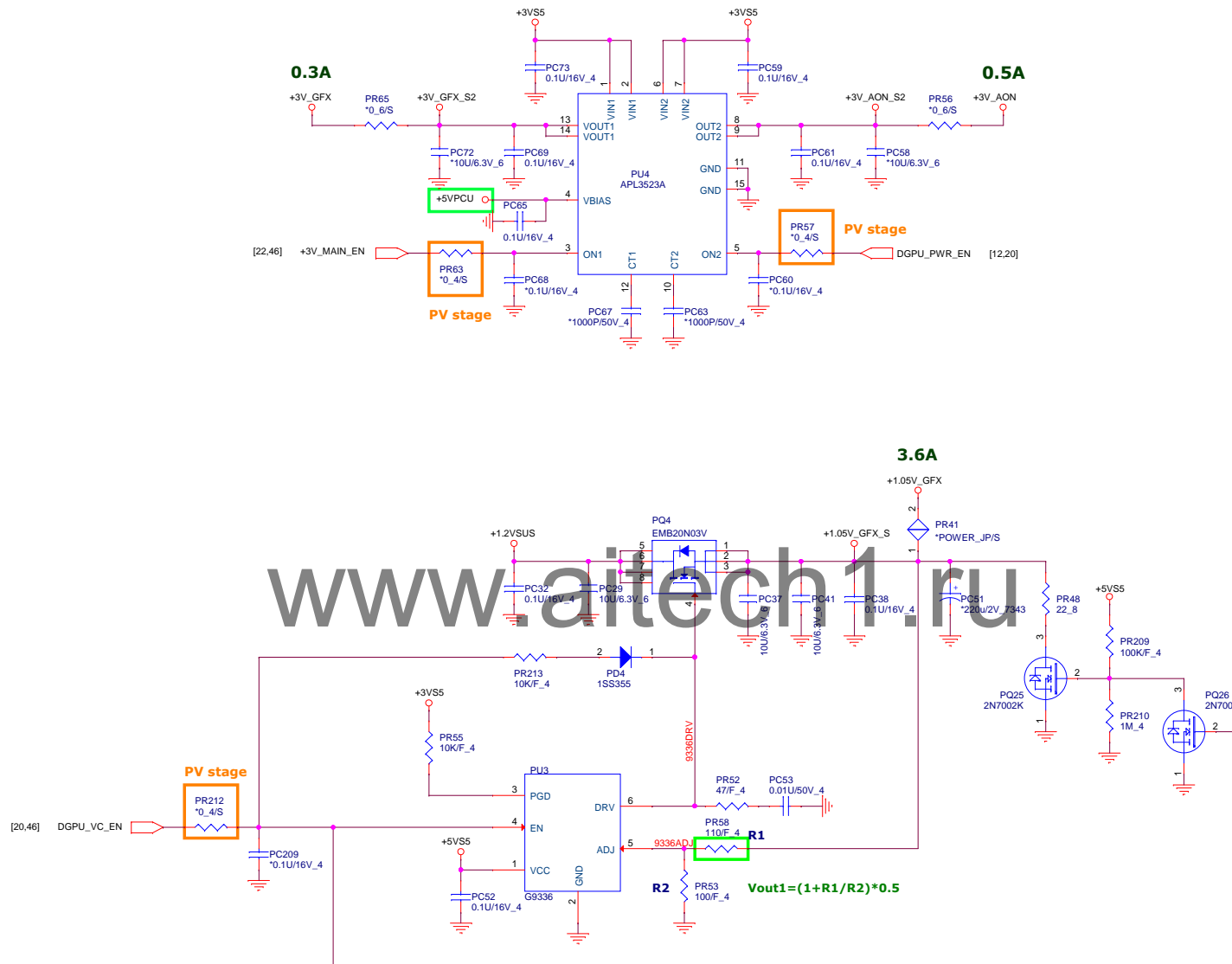
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

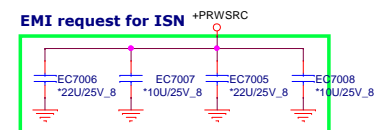
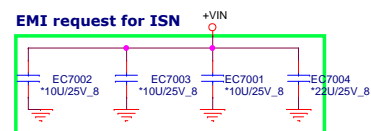
+3V	[2,4,10,13,15,21,25,27,29,30,32,33,35,41,46]
+5V	[26,27,29]
+VIN	[25,36,39,41,44,46,47,49]
+3VS5	[4,10,15,16,27,31,32,35,37,40,44,48]
+5VS5	[4,26,32,37,43,46,48]
+3VSUS	[29]
+5VPCU	[37,48]
+3VLAVCC	[33,34]





+VIN [25,36,39,41,44,46,47,49]
 +3VS5 [4,10,15,16,27,31,32,35,37,40,44,45]
 +5VS5 [4,26,32,37,43,45,47]
 +3V_GFX [19,21,22,46,47]
 +3V_AON [19,22,34]
 +1.2VSUS [3,6,17,18,38,40]
 +1.05V_GFX [19,21]





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